

# **An application note for an IGBT failure check process**

## **Precautions**

Due to the structure of the IGBT die, a press-pack IGBT is both pressure and electrostatic discharge (ESD) sensitive. Non-homogeneous clamping or over clamping pressure on a device can potentially result in direct damage of the silicon or deterioration of the operating capability of the device.

Secondly, due to the MOSFET gate structure, an IGBT is sensitive to ESD. Personnel handling the device without taking appropriate ESD precautions may cause catastrophic damage to the device, due to the uncontrolled static discharge/ induced high voltages.

## **Failure sources and category**

There are many causes of a press pack IGBT failure beyond the scope of this document, however some of the common failure mechanisms are described below:

1. Gate/Emitter short circuit (low impedance) - This type of failure is typically caused by the failure of the gate trigger circuit or due to loss of external control. Failure due to electrostatic damage or non-homogeneous or over clamping is also a possible cause of failure.
2. Collector/ Emitter short circuit - This type of failure is typically caused by an IGBT forward overvoltage failure or anti-parallel diode reverse overvoltage or due to loss of gate control. Failure due to non-homogeneous clamping or over clamping is also a possible cause of failure.
3. Three terminal short circuit - This type of failure is normally caused by dynamic switching failure when the device operates outside of the SOA limit or a consequential failure due to loss or interruption of the gate trigger.
4. Degraded blocking capability and/or high gate leakage - This is likely to have resulted from excessive junction temperature or from operation beyond the reverse bias operating area (RBSOA) limits or exceeding the voltage ratings.

With any of the symptoms above, the device should not be re-used.

## Gate check

It is simple to use a curve tracer to quickly check the gate / emitter characteristic. Taking the Tektronix 576 type curve tracer as an example, the test procedure is given in the following process:

1. The IGBT must be uniformly clamped across the whole electrode surface and the clamp force must be within the datasheet limits.
2. Connect the emitter and the gate pin of IGBT to **C** and **E** plugs in the probe terminals of the curve tracer as shown in figure 1 and 2.
3. Set **Polarity** dial to **AC**
4. Switch **Left-Off-Right** to left or right according to the side of probe leads connected
5. Set **Max Peak Volts** to 15V
6. Set **Vertical Sensitivity** to 500 $\mu$ A/div
7. Set **Horizontal Sensitivity** to 5V/div
8. Turn **Variable Collector Supply** dial to maximum
9. Check the gate waveform on the screen. If the gate is within specification, a waveform with a threshold current spike will appear. If the gate is a short circuit, only a straight line along the vertical axis will be seen. Figure 3 shows a typical example of a gate waveform:

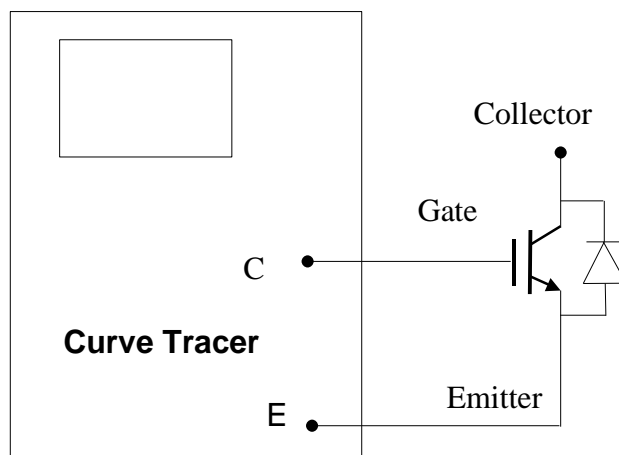


Figure 1: Schematic of the gate test

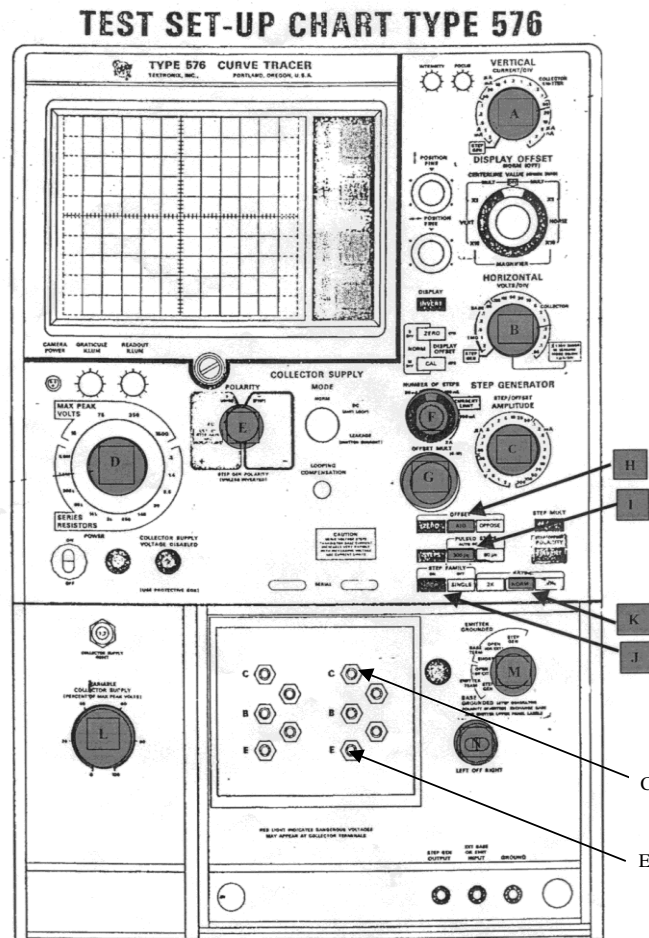


Figure 2: Front panel of the curve tracer

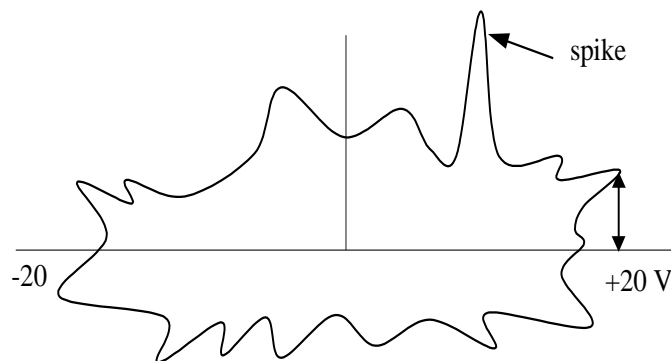


Figure 3: Gate current waveform

### **Forward voltage blocking check**

Normally, a press-pack IGBT is unable to block the forward voltage once it has failed during dynamic switching. The blocking failure can be checked using a curve tracer. It must be noted however that the peak voltage of the curve tracer is limited to approximately 1800V so the full blocking capability of an IGBT cannot be tested with this equipment.

The procedure is given in the following process:

**Note that this test involves potentially lethal voltages and should only be carried out by suitable qualified personnel.**

1. Make sure the emitter to collector pin is short circuit.
2. The IGBT must be uniformly clamped across the whole electrode surface and the clamp force must be within the datasheet limits.
3. Connect the emitter and the collector pin of IGBT to **C** and **E** plugs in the probe terminals of the curve tracer as shown in figure 4.
4. Set **Polarity** dial to **NPN**
5. Switch **Left-Off-Right** to left or right according to the side of probe leads connected
6. Set **Max Peak Volts** to 1500V
7. Set **Horizontal Sensitivity** to 200V/div
8. Set **Vertical Sensitivity** to 2mA/div
9. Press safety interlock button to switch on the high voltage output (red light is indicating)
10. Slowly turn the **Variable Collector Supply** dial to increase the blocking voltage. If the device still blocks voltage, the leakage current waveform should be less than 20mA as shown in figure 5, otherwise the device is likely to fail blocking.

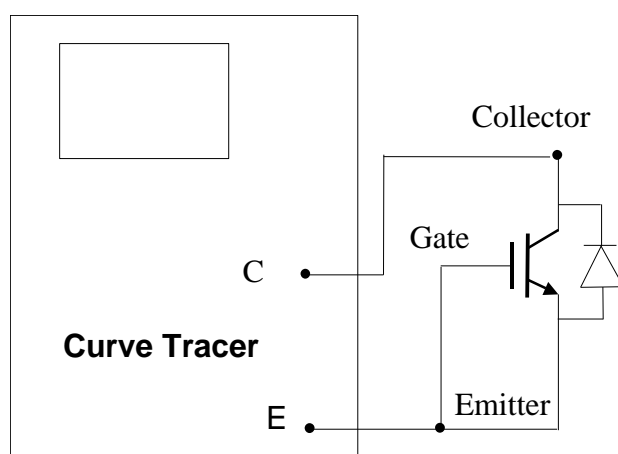


Figure 4: Schematic of the blocking test

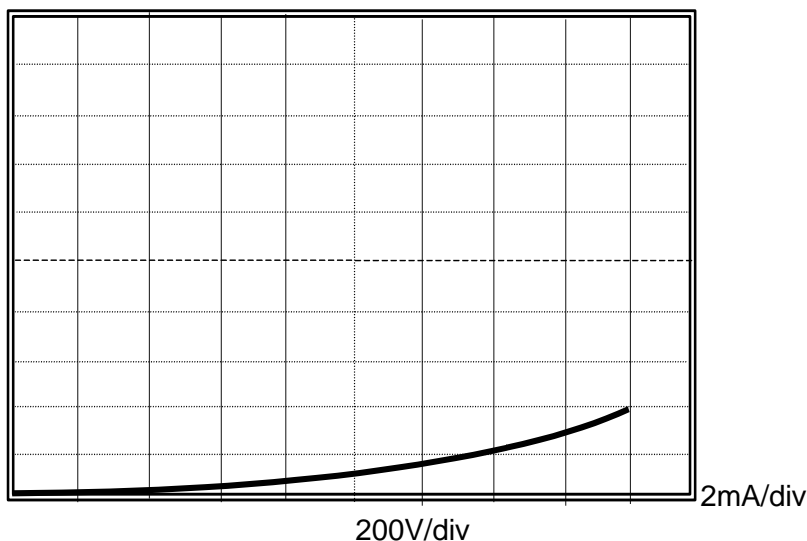


Figure 5: Schematic of a typical blocking leakage current waveform

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