

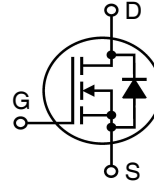
Polar3™ HiperFET™

Power MOSFET

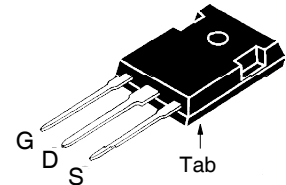
IXFH42N60P3

$$\begin{aligned} V_{DSS} &= 600V \\ I_{D25} &= 42A \\ R_{DS(on)} &\leq 185m\Omega \end{aligned}$$

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Rectifier



TO-247



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	600	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	600	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}$	42	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	100	A
I_A	$T_C = 25^\circ\text{C}$	21	A
E_{AS}	$T_C = 25^\circ\text{C}$	1	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$	35	V/ns
P_D	$T_C = 25^\circ\text{C}$	830	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
M_d	Mounting Torque	1.13 / 10	Nm/lb.in
Weight		6	g

Features

- International Standard Package
- Fast Intrinsic Rectifier
- Avalanche Rated
- Low $R_{DS(ON)}$ and Q_G
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- Laser Drivers
- AC and DC Motor Drives
- Robotics and Servo Controls

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 1mA$	600		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 4mA$	3.0		5.0 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			25 μA 1.5 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			185 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}, I_D = 0.5 \cdot I_{D25}$, Note 1	25	42	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		5150	pF
C_{oss}			500	pF
C_{rss}			2.8	pF
R_{Gi}	Gate Input Resistance		1.0	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		32	ns
t_r			23	ns
$t_{d(off)}$			60	ns
t_f			17	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		78	nC
Q_{gs}			23	nC
Q_{gd}			20	nC
R_{thJC}				0.15 $^\circ\text{C/W}$
R_{thCS}			0.21	$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			42 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			168 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{V}$, Note 1			1.3 V
t_{rr}	$I_F = 21\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			250 ns
I_{RM}			12.4	A
Q_{RM}			1.4	μC

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

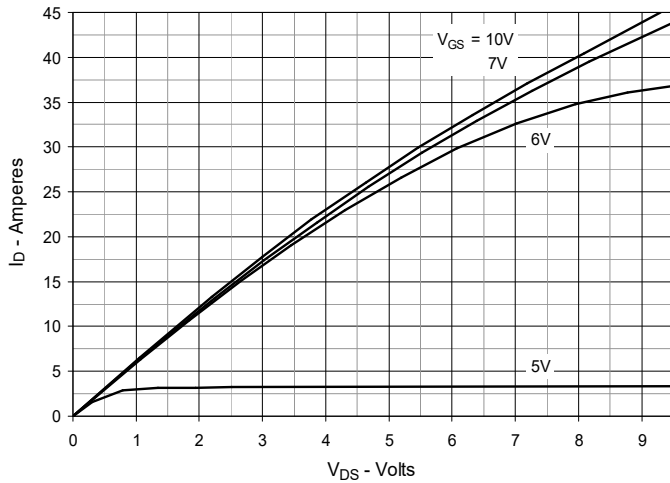
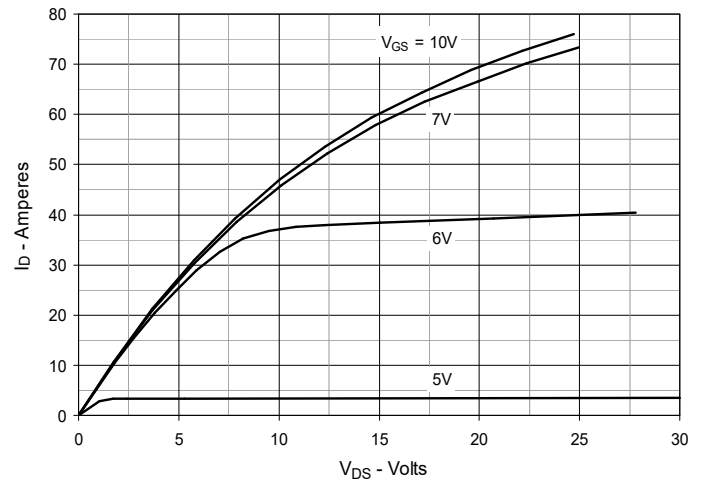
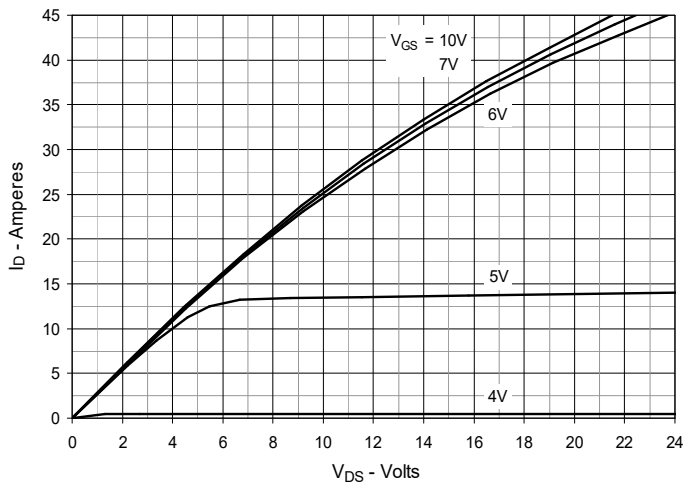
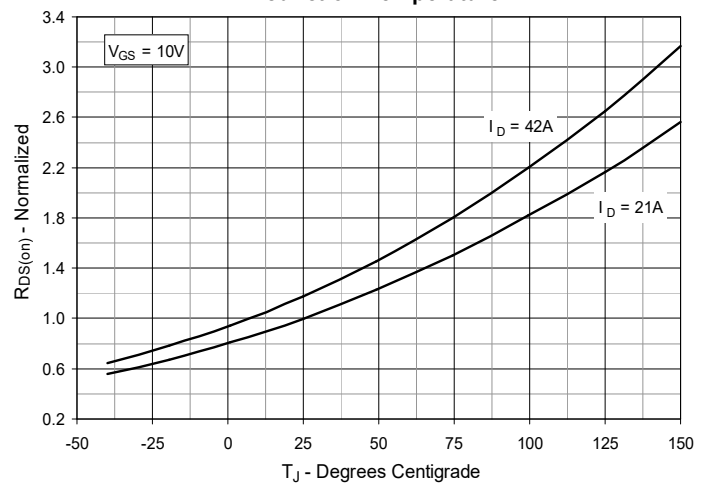
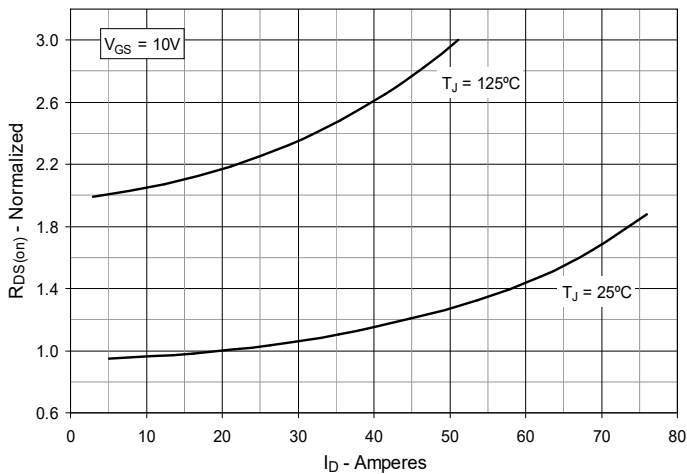
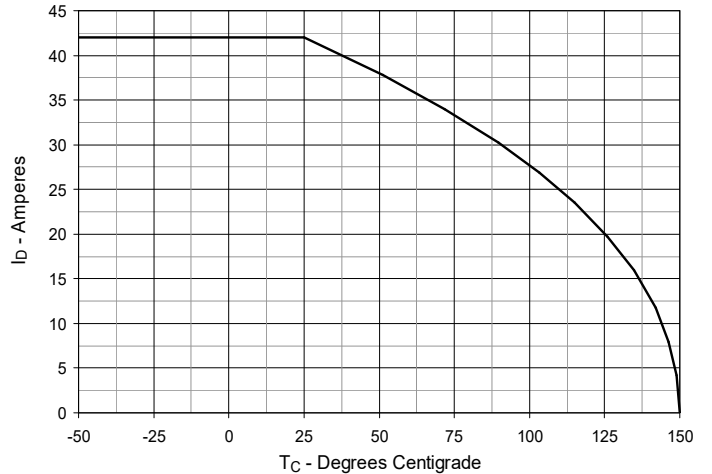
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 21\text{A}$ Value vs. Junction Temperature

Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 21\text{A}$ Value vs. Drain Current

Fig. 6. Maximum Drain Current vs. Case Temperature


Fig. 7. Input Admittance

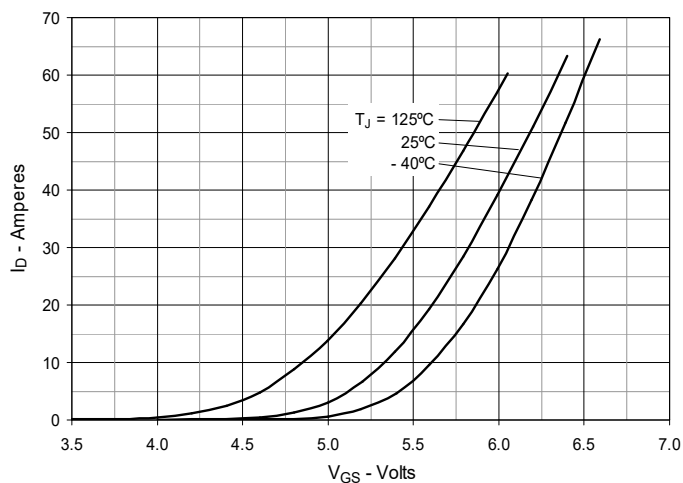


Fig. 8. Transconductance

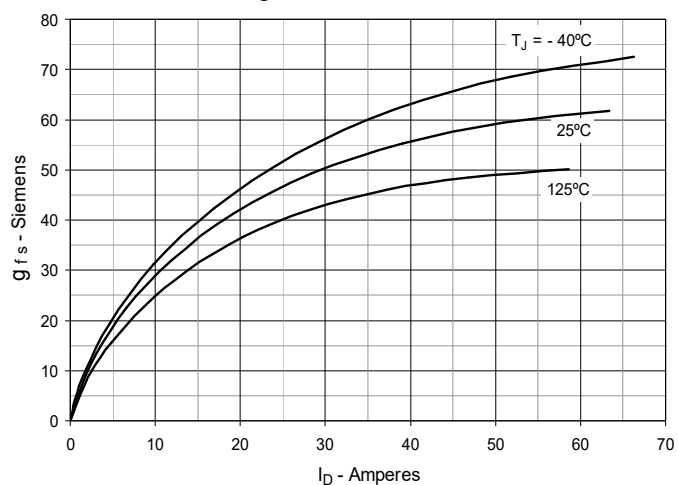


Fig. 9. Forward Voltage Drop of Intrinsic Diode

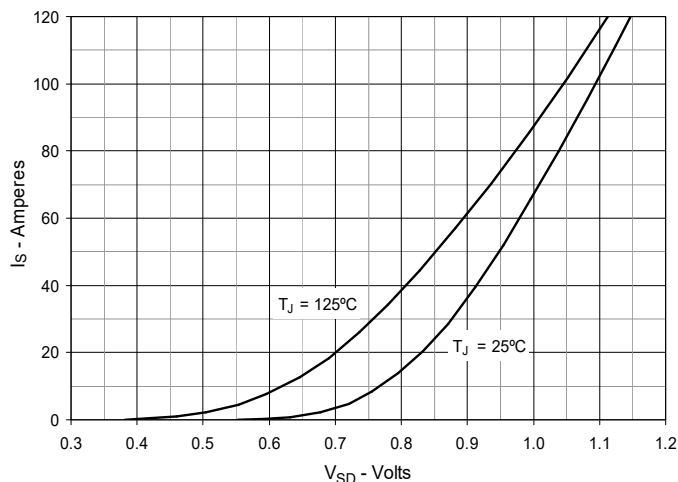


Fig. 10. Gate Charge

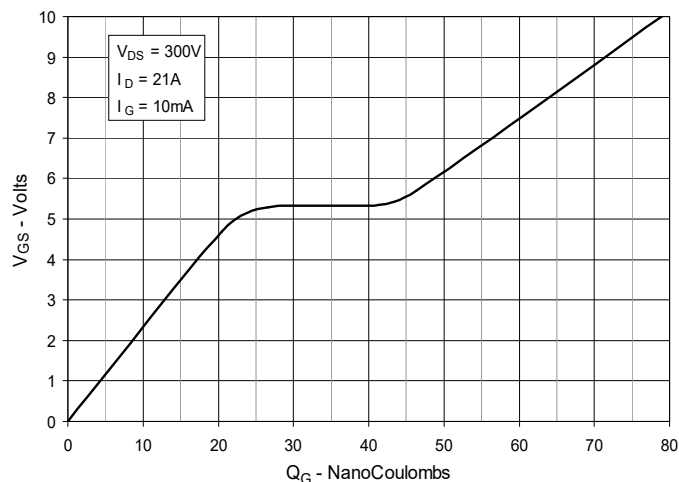


Fig. 11. Capacitance

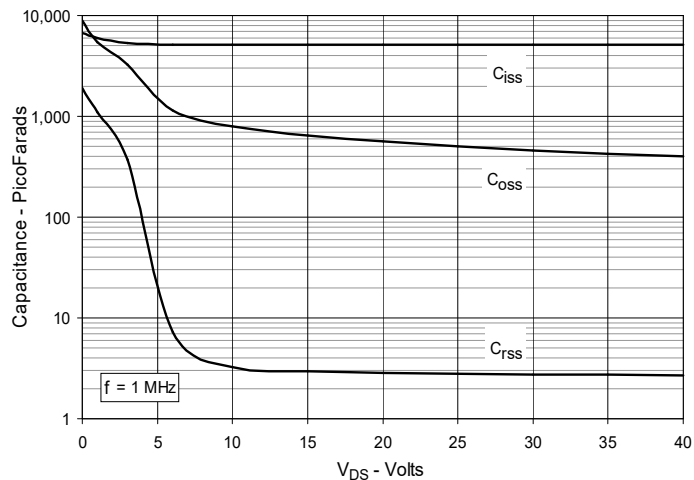


Fig. 12. Forward-Bias Safe Operating Area

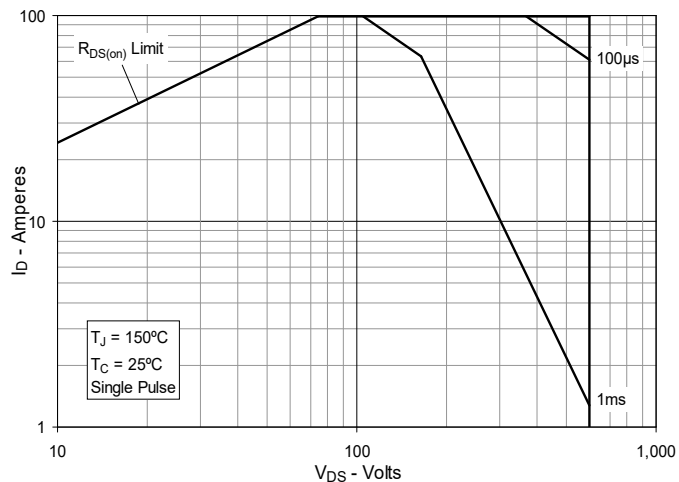
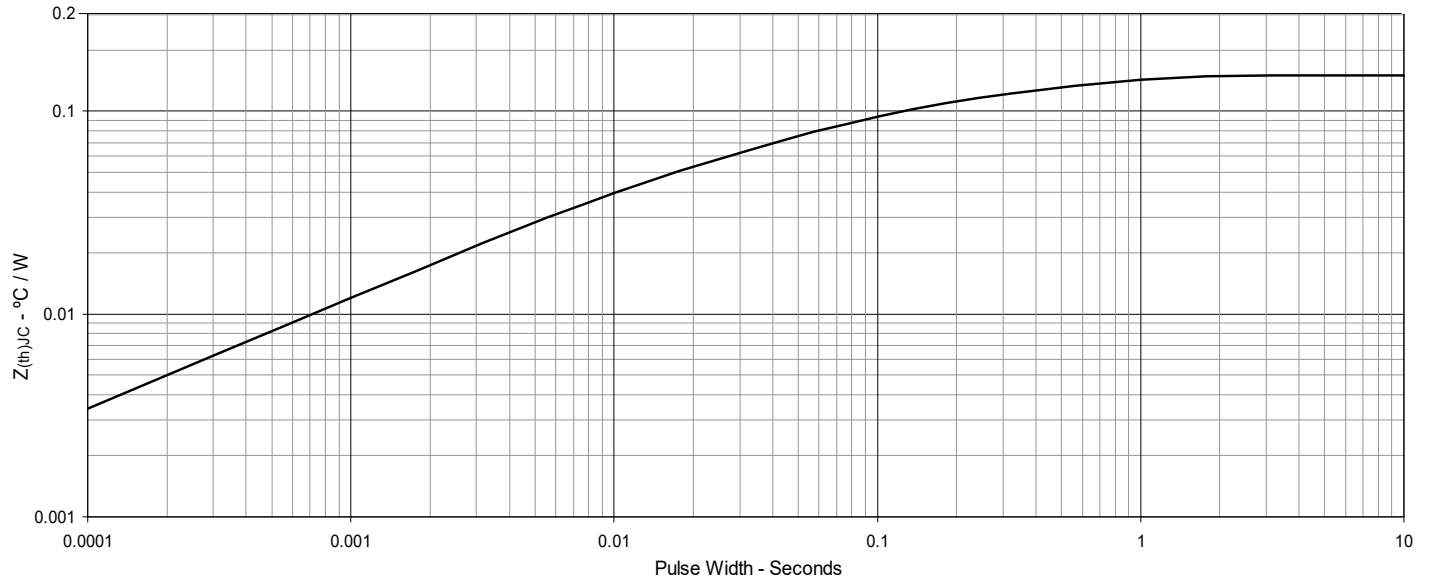
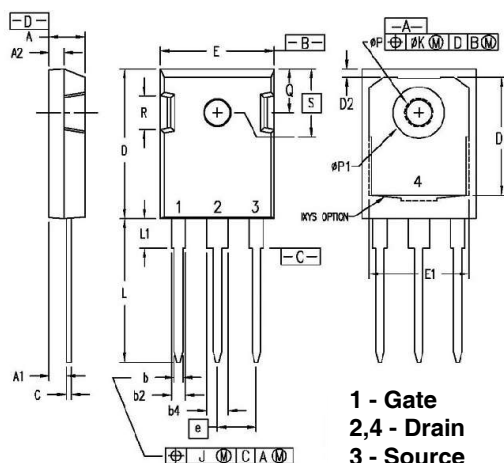


Fig. 13. Maximum Transient Thermal Impedance



TO-247 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.545	.565	13.84	14.35
e	.215 BSC		5.45 BSC	
J	--	.010	--	0.25
K	--	.025	--	0.64
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
ØP	.140	.144	3.55	3.65
ØP1	.275	.290	6.99	7.37
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.242 BSC		6.15 BSC	

NOTE: This drawing will meet all dimensions requirement of JEDEC outlines TO-247 AD (R-PSIP-F3)

