

Parameter	Rating	Units
Blocking Voltage	400	V <sub>p</sub>
Load Current	500	mA <sub>rms</sub> / mA <sub>DC</sub>
On-Resistance (max)	6	Ω
Input Voltage to operate	5-12	V

## Features

- Voltage-Controlled Operation
- Matches Popular Reed Relay Pin-Out
- 3750V<sub>rms</sub> Input/Output Isolation
- 100% Solid State
- No EMI/RFI Generation
- Immune to Radiated EM Fields
- 4-Pin DIP Package

## Applications

- Security
  - Passive Infrared Detectors (PIR)
  - Data Signalling
  - Sensor Circuitry
- Telecommunications
- Instrumentation
- Multiplexers
- Data Acquisition
- Electronic Switching
- I/O Subsystems
- Energy Meters
- Medical Equipment—Patient/Equipment Isolation
- Industrial Controls

## Description

The CPC1215 is a voltage-controlled, single-pole, normally open (1-Form-A), optically coupled solid state relay in a 4-pin Dual In-line Package (DIP). IXYS Integrated Circuits Division's patented OptoMOS architecture makes available the optically coupled technology necessary to activate the output's efficient MOSFET switches while providing a 3750V<sub>rms</sub> input-to-output isolation barrier. Control of the isolated output is accomplished by means of a highly efficient infrared LED at the input while the internal resistor in series with the LED enables the input's voltage-controlled operation.

Because the input is solid state there is no need for snubbers or "catch" diodes to suppress the inductive flyback transient voltage normally associated with EMR coils.

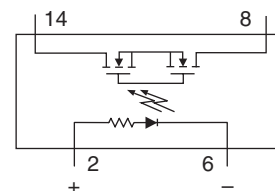
## Approvals

- TUV EN 62368-1: Certificate # B 082667 0008

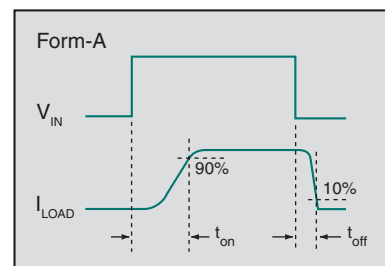
## Ordering Information

Part #	Description
CPC1215G	4-Pin DIP (14-Pin Body) (25/tube)

## Pin Configuration



## Switching Characteristics of Normally Open Devices



### Absolute Maximum Ratings @ 25°C

Parameter	Ratings	Units
Blocking Voltage	400	V <sub>P</sub>
Reverse Input Voltage	5	V
Input Control Voltage	15	V
Input Power Dissipation	225	mW
Total Power Dissipation <sup>1</sup>	1600	mW
Isolation Voltage, Input to Output	3750	V <sub>rms</sub>
ESD, Human Body Model	8	kV
Operational Temperature, Ambient	-40 to +85	°C
Storage Temperature	-40 to +125	°C

<sup>1</sup> Derate output power linearly 16.6 mW / °C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

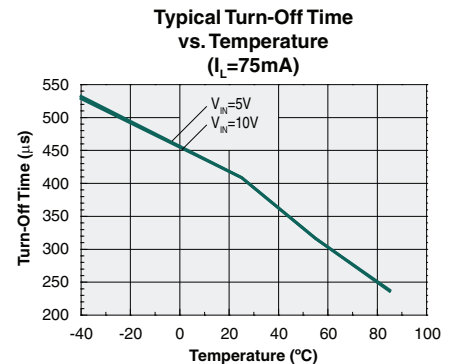
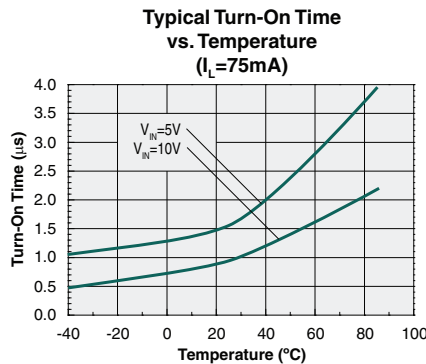
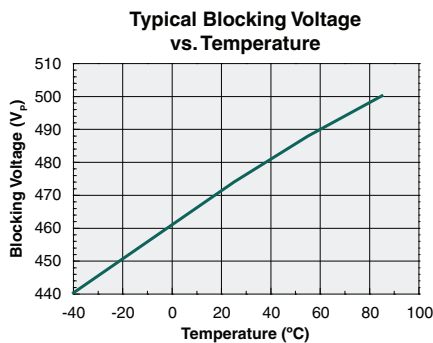
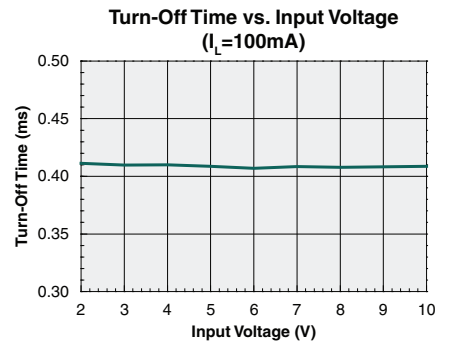
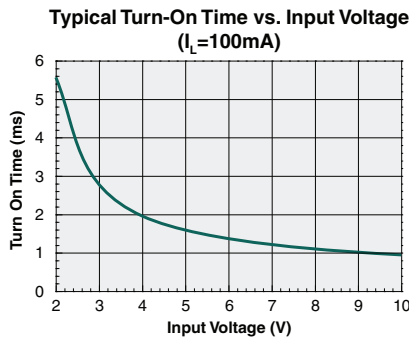
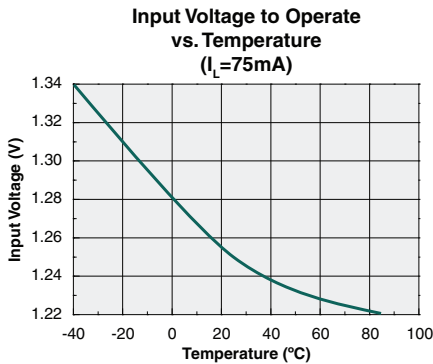
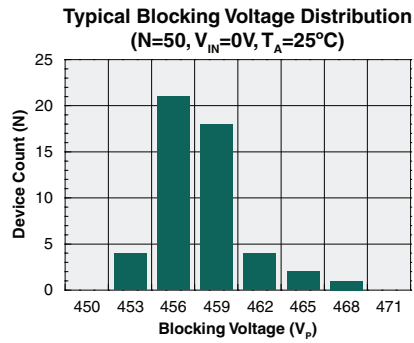
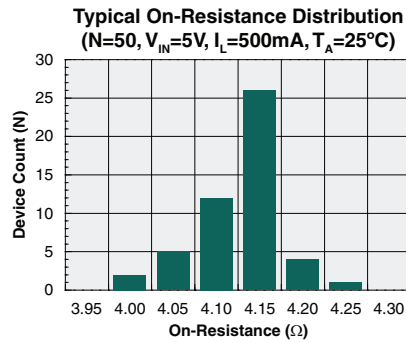
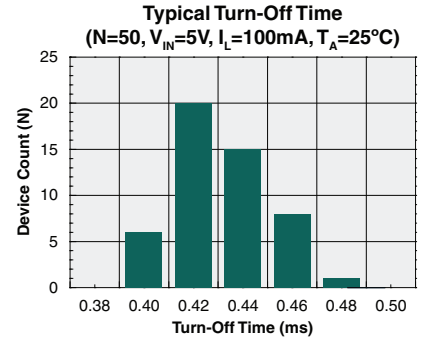
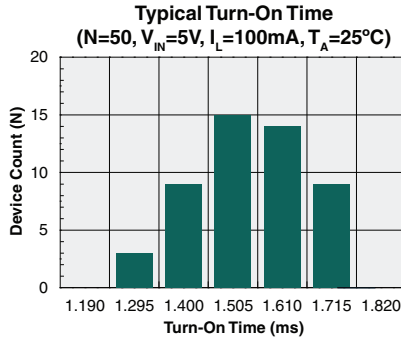
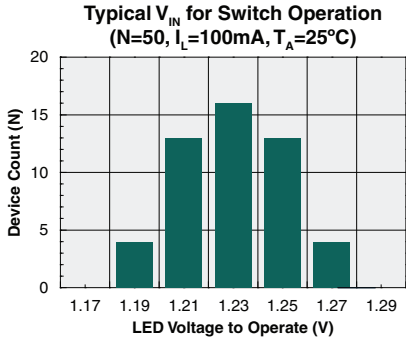
Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

### Electrical Characteristics @ 25°C

Parameter	Conditions	Symbol	Min	Typ	Max	Units
<b>Output Characteristics</b>						
Blocking Voltage	I <sub>L</sub> =1μA,	V <sub>DRM</sub>	400	-	-	V
Load Current						
Continuous	V <sub>IN</sub> =5V	I <sub>L</sub>	-	-	500	mA <sub>rms</sub> / mA <sub>DC</sub>
Peak	t=10ms	I <sub>LPK</sub>	-	-	±1.5	A <sub>P</sub>
On-Resistance <sup>1</sup>	I <sub>L</sub> =500mA	R <sub>ON</sub>	-	4.15	6	Ω
Off-State Leakage Current	V <sub>L</sub> =400V <sub>P</sub>	I <sub>LEAK</sub>	-	0.009	1	μA
Switching Speeds						
Turn-On (Output Closed)	V <sub>IN</sub> =5V, V <sub>L</sub> =10V	t <sub>on</sub>	-	1.55	5	ms
Turn-Off (Output Open)		t <sub>off</sub>	-	0.42	3	
Output Capacitance	V <sub>IN</sub> =0V, V <sub>L</sub> =50V, f=1MHz	C <sub>OUT</sub>	-	18	-	pF
<b>Input Characteristics</b>						
Input Control Voltage						
Recommended Operating Range	I <sub>L</sub> =500mA	V <sub>IN</sub>	5	-	12	V
Output Closed			-	-	3.75	
Output Open			1	-	-	
Reverse Input Current	V <sub>IN</sub> =-5V	I <sub>R</sub>	-	-	10	μA
Input Resistor	-	-	900	1000	1100	Ω
<b>Common Characteristics</b>						
Capacitance, Input to Output	V <sub>IO</sub> =0V, f=1MHz	C <sub>IO</sub>	-	1	-	pF

<sup>1</sup> Measurement taken within 1 second of on-time.

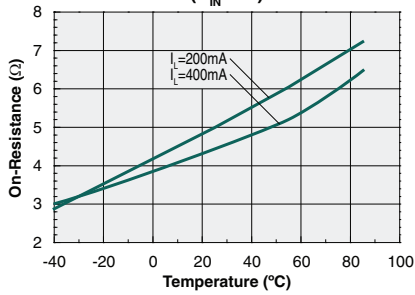
**PERFORMANCE DATA\***



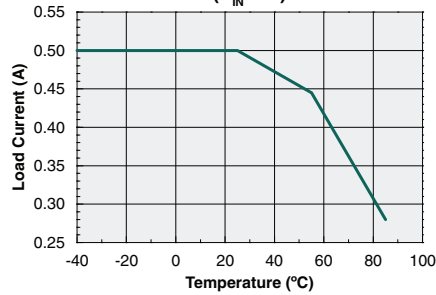
\*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C.

**PERFORMANCE DATA\***

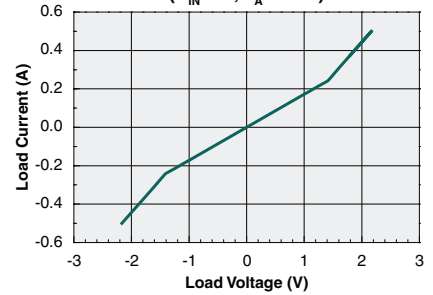
**Typical On-Resistance vs. Temperature**  
( $V_{IN}=5V$ )



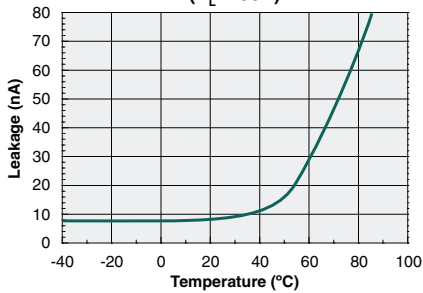
**Load Current vs. Temperature**  
( $V_{IN}=5V$ )



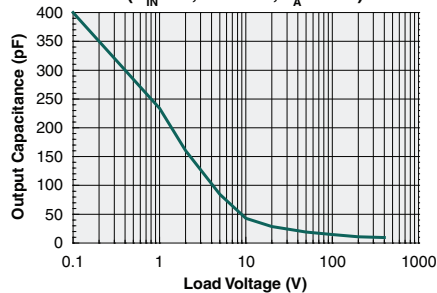
**Typical Load Current vs. Load Voltage**  
( $V_{IN}=5V, T_A=25°C$ )



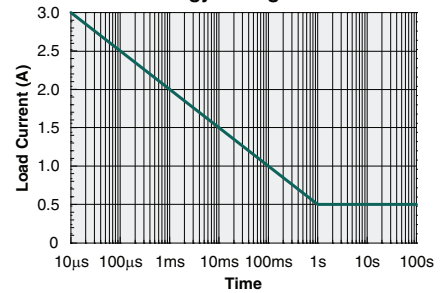
**Typical Leakage vs. Temperature**  
Measured Across Pins 14 & 8  
( $V_L=400V$ )



**Output Capacitance vs. Load Voltage**  
( $V_{IN}=0V, f=1MHz, T_A=25°C$ )



**Energy Rating Curve**



\*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C.

## Manufacturing Information

### ESD Sensitivity



This product is ESD Sensitive, and should be handled according to the industry standard **JESD-625**.

### Soldering Profile

For through-hole devices, the maximum pin temperature and maximum dwell time through all solder waves is provided in the table below. Dwell time is the interval beginning when the pins are initially immersed into the solder wave until they exit the solder wave. For multiple waves, the dwell time is from entering the first wave until exiting the last wave. During this time, pin temperatures must not exceed the maximum temperature given in the table below. Body temperature of the device must not exceed the limit shown in the table below at any time during the soldering process.

Device	Maximum Pin Temperature	Maximum Body Temperature	Maximum Dwell Time	Wave Cycles
CPC1215G	260°C	245°C	10 seconds*	1

\*Total cumulative duration of all waves.

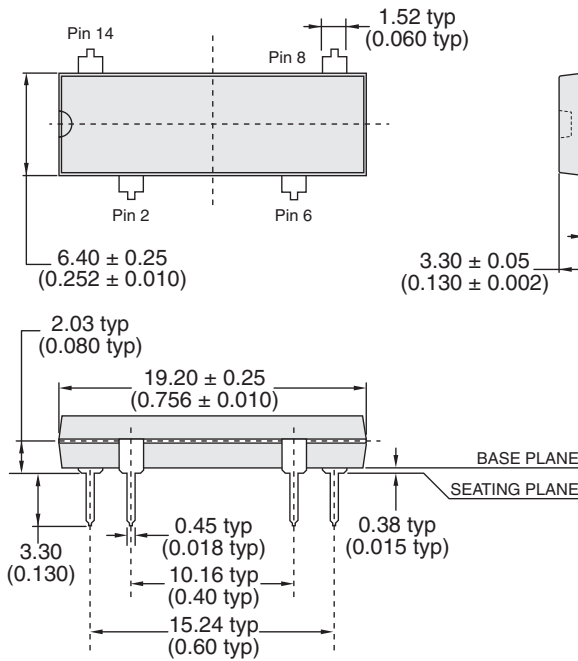
### Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

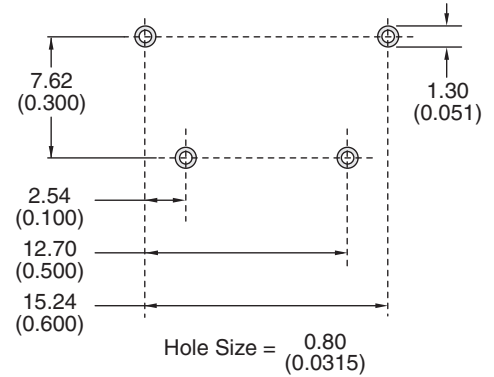


MECHANICAL DIMENSIONS

CPC1215G



PCB Hole Pattern



DIMENSIONS  
mm  
(inches)

NOTES:

1. All dimensions are in mm (inches).
2. Coplanarity = 0.102 (0.004) max.
3. Leadframe thickness does not include solder plating (1000 μinches max).

For additional information please visit our website at: <https://www.ixysic.com>