

## Characteristics

Parameter	Rating	Units
Blocking Voltage	400	$V_P$
Load Current, $T_A=25^\circ\text{C}$ :		$A_{\text{rms}} / A_{\text{DC}}$
With $5^\circ\text{C/W}$ Heat Sink	3.35	
No Heat Sink	1.35	
On-Resistance (max)	0.85	$\Omega$
Thermal Impedance, Junction-to-Case, $\theta_{\text{JC}}$	0.35	$^\circ\text{C/W}$

## Features

- $3.35A_{\text{rms}}$  Load Current with  $5^\circ\text{C/W}$  Heat Sink
- Low  $0.85\Omega$  On-Resistance
- $400V_P$  Blocking Voltage
- $2500V_{\text{rms}}$  Input/Output Isolation
- Low Thermal Impedance:  $\theta_{\text{JC}} = 0.35^\circ\text{C/W}$
- Isolated, Low Thermal Impedance Ceramic Pad for Heat Sink Applications
- Low Drive Power Requirements
- No EMI/RFI Generation
- Flammability Rating UL 94 V-0

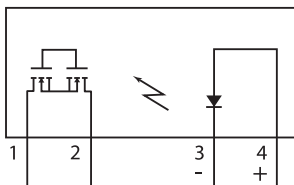
## Applications

- Industrial Controls / Motor Control
- Robotics
- Medical Equipment—Patient/Equipment Isolation
- Instrumentation
- Multiplexers
- Data Acquisition
- Electronic Switching
- I/O Subsystems
- Meters (Watt-Hour, Water, Gas)
- Transportation Equipment

## Approvals

- UL 508 Recognized Component: File E69938

## Pin Configuration



## Description

IXYS Integrated Circuits brings OptoMOS® technology, reliability and compact size to a new family of high power Solid State Relays.

As part of this family, the CPC1967J single-pole normally open (1-Form-A) Solid State Power Relay is rated for up to  $3.35A_{\text{rms}}$  continuous load current with a  $5^\circ\text{C/W}$  heat sink.

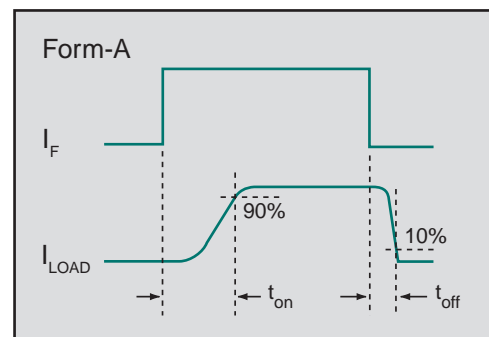
The CPC1967J employs optically coupled MOSFET technology to provide  $2500V_{\text{rms}}$  of input to output isolation. The optically coupled outputs, that use patented OptoMOS architecture, are controlled by a highly efficient infrared LED. The combination of low on-resistance and high load current handling capability makes this relay suitable for a variety of high performance switching applications.

The unique i4-PAC package pioneered by IXYS enables Solid State Relays to achieve the highest load current and power ratings. This package features a unique IXYS process where the silicon chips are soft soldered onto the Direct Copper Bond (DCB) substrate instead of the traditional copper leadframe. The DCB ceramic, the same substrate used in high power modules, not only provides  $2500V_{\text{rms}}$  isolation, but also very low junction-to-case thermal impedance ( $0.35^\circ\text{C/W}$ ).

## Ordering Information

Part	Description
CPC1967J	i4-PAC Package (25 per tube)

## Switching Characteristics



## 1 Specifications

### 1.1 Absolute Maximum Ratings @ 25°C

Parameter	Symbol	Rating	Unit
Blocking Voltage	$V_L$	400	$V_P$
Reverse Input Voltage	$V_R$	5	V
Input Control Current, Continuous Peak (10ms)	$I_F$	100	mA
		1	A
Input Power Dissipation	$P_{IN}$	150	mW
Isolation Voltage (Input to Output)	$V_{ISO}$	2500	$V_{rms}$
Operating Temperature	$T_A$	-40 to +85	°C
Storage Temperature	-	-40 to +125	°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.

### 1.2 Electrical Characteristics @ 25°C

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
<b>Output Characteristics</b>						
Load Current <sup>1</sup> Peak Continuous Continuous Continuous	$t \leq 10ms$	$I_L$	-	-	15	$A_P$
	No Heat Sink				1.35	
	$T_C = 25^\circ C$	$I_{L(99)}$	-	-	13.15	$A_{rms} / A_{DC}$
	$T_C = 99^\circ C$				1.5	
On-Resistance <sup>2</sup>	$I_F = 10mA, I_L = 1A$	$R_{ON}$	-	0.7	0.85	$\Omega$
Off-State Leakage Current	$V_L = 400V_P$	$I_{LEAK}$	-	-	1	$\mu A$
Switching Speeds Turn-On Turn-Off	$I_F = 10mA, V_L = 10V$	$t_{on}$	-	5	20	ms
		$t_{off}$	-	0.13	5	
Output Capacitance	$I_F = 0mA, V_L = 25V, f = 1MHz$	$C_{out}$	-	470	-	pF
<b>Input Characteristics</b>						
Input Control Current to Activate <sup>3</sup>	$I_L = 1A$	$I_F$	-	-	10	mA
Input Control Current to Deactivate	-	$I_F$	0.6	-	-	mA
Input Voltage Drop	$I_F = 10mA$	$V_F$	0.9	1.35	1.56	V
Reverse Input Current	$V_R = 5V$	$I_R$	-	-	10	$\mu A$
<b>Input/Output Characteristics</b>						
Capacitance, Input-to-Output	$V_{IO} = 0V, f = 1MHz$	$C_{IO}$	-	1	-	pF

<sup>1</sup> Higher load currents possible with proper heat sinking.

<sup>2</sup> Measurement taken within 1 second of on-time.

<sup>3</sup> For applications requiring high temperature operation ( $T_C > 60^\circ C$ ) a minimum LED drive current of 20mA is recommended.

## 2 Thermal Characteristics

Parameter	Conditions	Symbol	Rating	Units
Thermal Impedance (Junction to Case)	-	$\theta_{JC}$	0.35	$^{\circ}\text{C}/\text{W}$
Thermal Impedance (Junction to Ambient)	Free Air	$\theta_{JA}$	33	$^{\circ}\text{C}/\text{W}$
Junction Temperature (Operating)	-	$T_J$	-40 to +100	$^{\circ}\text{C}$

### 2.1 Thermal Management

Device high current characterization was performed using Kunze heat sink KU 1-159, phase change thermal interface material KU-ALC 5, and transistor clip KU 4-499/1. This combination provided an approximate junction-to-ambient thermal impedance of  $12.5^{\circ}\text{C}/\text{W}$ .

### 2.2 Heat Sink Calculation

Higher load currents are possible by using lower thermal impedance heat sink combinations.

#### Heat Sink Rating

$$\theta_{CA} = \frac{(T_J - T_A) I_{L(99)}^2}{I_L^2 \cdot P_{D(99)}} - \theta_{JC}$$

$T_J$  = Junction Temperature ( $^{\circ}\text{C}$ ),  $T_J \leq 100^{\circ}\text{C}$  \*

$T_A$  = Ambient Temperature ( $^{\circ}\text{C}$ )

$I_{L(99)}$  = Load Current with Case Temperature @  $99^{\circ}\text{C}$  ( $A_{DC}$ )

$I_L$  = Desired Operating Load Current ( $A_{DC}$ ),  $I_L \leq I_{L(MAX)}$

$\theta_{JC}$  = Thermal Impedance, Junction to Case ( $^{\circ}\text{C}/\text{W}$ ) =  $0.35^{\circ}\text{C}/\text{W}$

$\theta_{CA}$  = Thermal Impedance of Heat Sink & Thermal Interface Material, Case to Ambient ( $^{\circ}\text{C}/\text{W}$ )

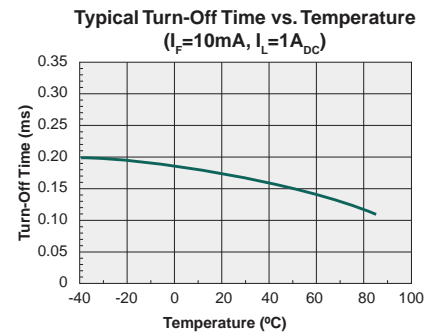
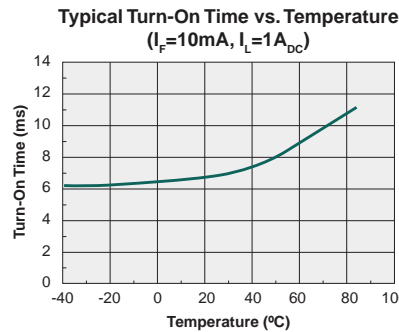
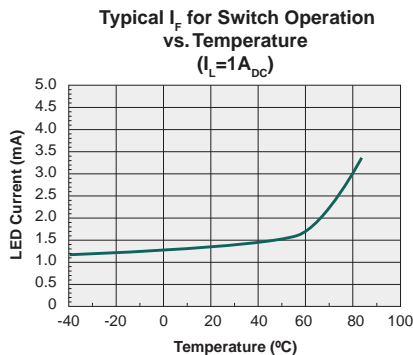
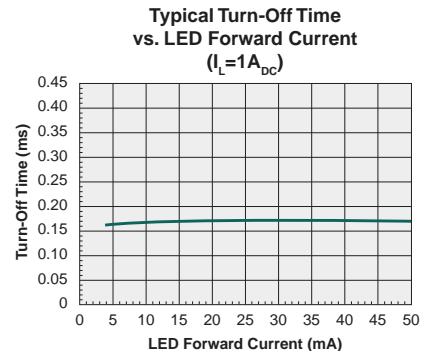
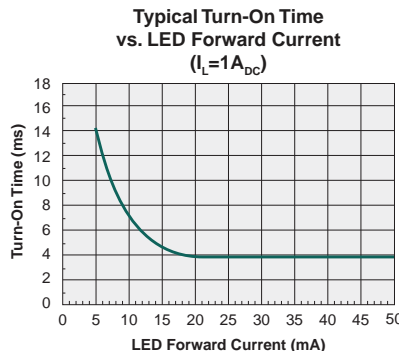
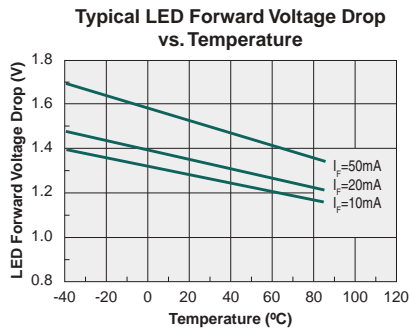
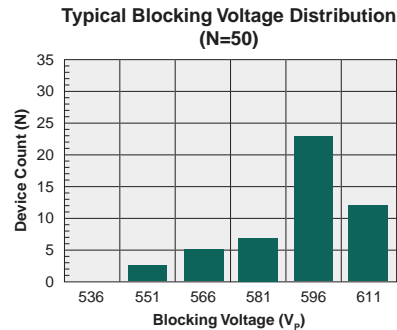
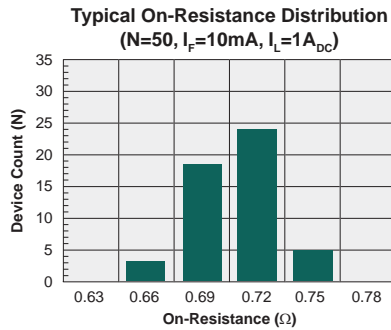
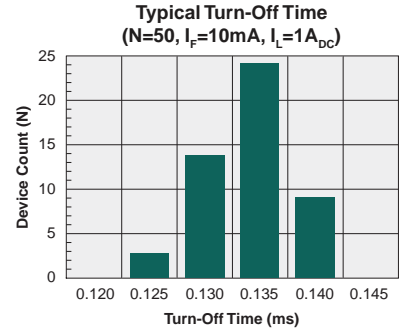
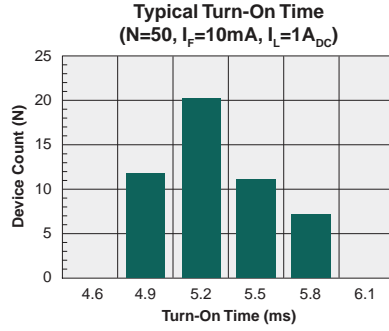
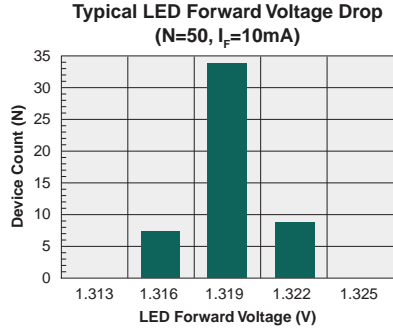
$P_{D(99)}$  = Maximum power dissipation with case temperature held at  $99^{\circ}\text{C}$  =  $2.86\text{W}$

\* Elevated junction temperature reduces semiconductor lifetime.

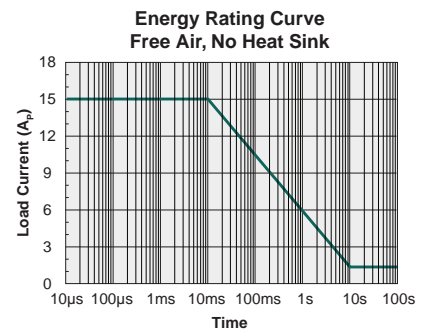
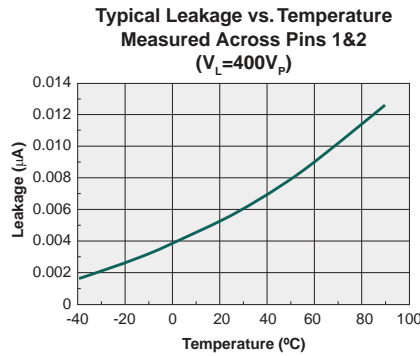
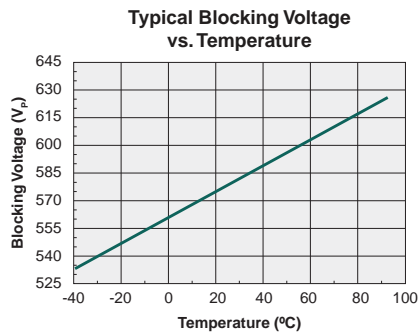
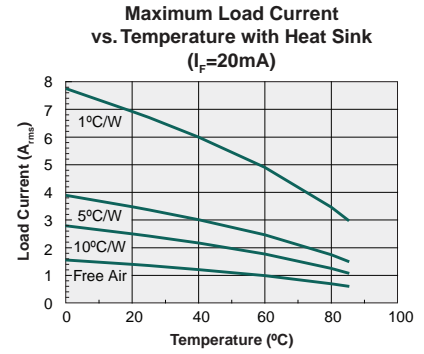
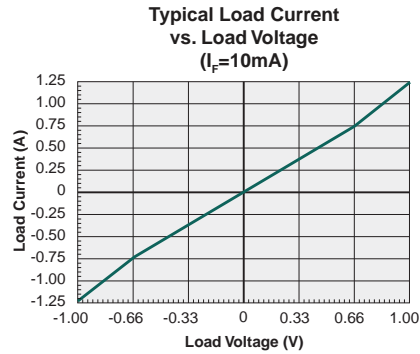
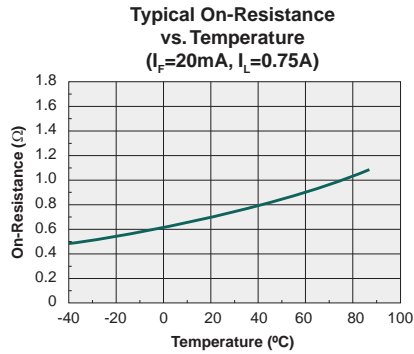
**NOTE:** The exposed surface of the DCB substrate is not to be soldered.

### 3 Performance Data\*

Unless otherwise specified, all performance data was acquired without the use of a heat sink.



\*Unless otherwise noted, data presented in these graphs is typical of device operation at 25 $^{\circ}\text{C}$ .



\*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C.

## 4 Manufacturing Information

### 4.1 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

### 4.2 Soldering Profile

For through-hole devices, the maximum and minimum peak solder temperature limits ( $T_p$ ) and the device maximum total dwell time through all solder waves is provided in the table below. Dwell time is the interval the device pins are at or above the minimum peak solder temperature. Body temperature of the device must not exceed the limit given in the table below at any time during the soldering process.

Device	Solder Temperature ( $T_p$ )		Body Temperature	Dwell Time	Wave Cycles
	Minimum	Maximum			
CPC1967J	235°C	260°C	245°C	10 seconds*	1

\*Total cumulative duration of all waves.

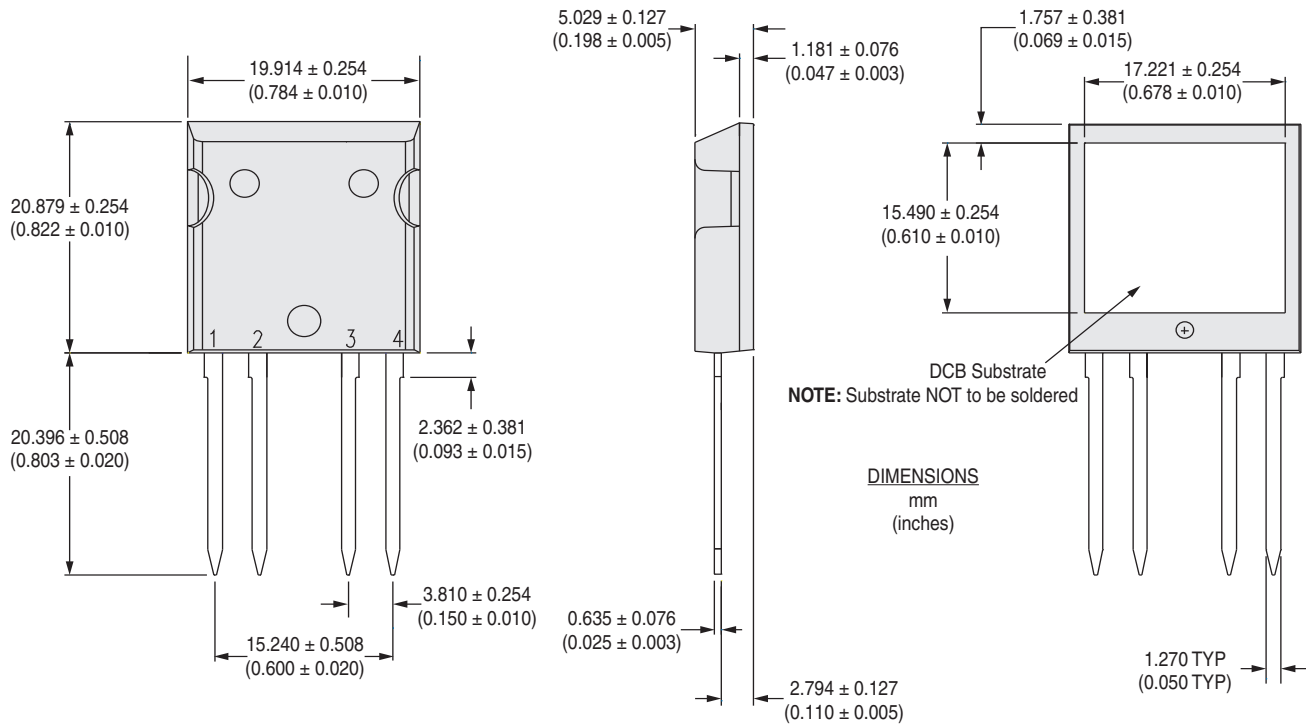
**NOTE:** The exposed surface of the DCB substrate must not be soldered.

### 4.3 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.



### 4.4 Mechanical Dimensions



**NOTES:**

1. Controlling dimension: Inches.
2. Metallized external surface of DCB substrate maintains 2500V<sub>rms</sub> isolation to device internal structure and all external pins.

For additional information please visit our website at: <https://www.ixysic.com>