IXYS
INTEGRATED CIRCUITS DIVISION

IXD_609SI
Automotive Grade
9-Ampere, Low-Side, Ultrafast MOSFET Drivers

Features

- AEC Q100 Qualified
- 9A Peak Source/Sink Drive Current
- Wide Operating Voltage Range: 4.5V to 35V
- AEC Q100 Grade 1 -40°C to +125°C Operating Temperature Range
- Logic Input Withstands Negative Swing of up to 5V
- Matched Rise and Fall Times
- Low Propagation Delay Time
- Low, 10μA Supply Current
- Low Output Impedance

Applications

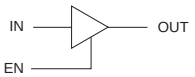
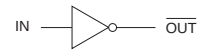
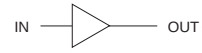
- Automotive DC/DC Regulators
- Electronic Power Steering
- Electric Vehicle Power Train Drives
- Brushless DC Motors

Description

The IXD_609SI is an automotive grade, high-speed gate driver that is qualified according to AEC Q100 standards. The IXD_609SI output can source and sink 9A of peak current, while producing rise and fall times of less than 45ns. Both the output and input are rated to 35V. The input is virtually immune to latch-up, and proprietary circuitry eliminates cross conduction and "shoot-through." The IXD_609SI has a Grade 1, -40°C to +125°C ambient operating temperature range.

The IXDD609SI is configured as a non-inverting driver with an enable, the IXDN609SI is configured as a non-inverting driver, and the IXDI609SI is configured as an inverting driver. The AEC Q100 qualified IXD_609SI is available in an 8-pin Power SOIC package with an exposed metal back.

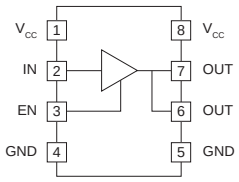
Ordering Information

Part Number	Logic Configuration	Package Type	Packing Method	Quantity
IXDD609SI		8-Pin Power SOIC with Exposed Metal Back	Tube	100
IXDD609SITR			Tape & Reel	2000
IXDI609SI			Tube	100
IXDI609SITR			Tape & Reel	2000
IXDN609SI			Tube	100
IXDN609SITR			Tape & Reel	2000

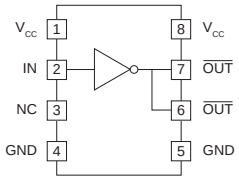
1 Specifications

1.1 Pin Configurations

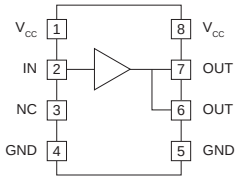
IXDD609SI



IXDI609SI



IXDN609SI



1.2 Pin Definitions

Pin Name	Description
IN	Logic Input
EN	Output Enable - Drive pin low to disable output, and force output to a high impedance state
OUT	Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
$\overline{OUT}$	Inverted Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
V_{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference for the device
NC	Not connected

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V_{CC}	-0.3	40	V
Input Voltage	V_{IN}, V_{EN}	-5	V_{CC}+0.3	V
Output Current	I_{OUT}	-	±9	A
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

Unless stated otherwise, absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Range	Units
Supply Voltage	V_{CC}	4.5 to 35	V
Operating Temperature Range	T_A	-40 to +125	°C

1.5 Electrical Characteristics: T_A = 25°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V (unless otherwise noted).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.0	-	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	-	0.8	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	-	±10	µA
EN Input Voltage, High	IXDD609SI only	V_{ENH}	2/3V_{CC}	-	-	V
EN Input Voltage, Low	IXDD609SI only	V_{ENL}	-	-	1/3V_{CC}	
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	0.6	1	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	0.4	0.8	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	±2	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	22	35	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	15	25	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	40	60	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	42	60	
Enable to Output-High Delay Time (IXDD609SI Only)	V_{CC}=18V	t_{ENOH}	-	25	60	
Disable to High Impedance State Delay Time (IXDD609SI Only)	V_{CC}=18V	t_{DOLD}	-	35	60	
Enable Pull-Up Resistor	-	R_{EN}	-	200	-	kΩ
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	1	2	mA
	V_{CC}=18V, V_{IN}=0V		-	<1	10	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	<1	10	

1.6 Electrical Characteristics: T_A = - 40°C to +125°C

Test Conditions: 4.5V ≤ V_{CC} ≤ 35V unless otherwise noted.

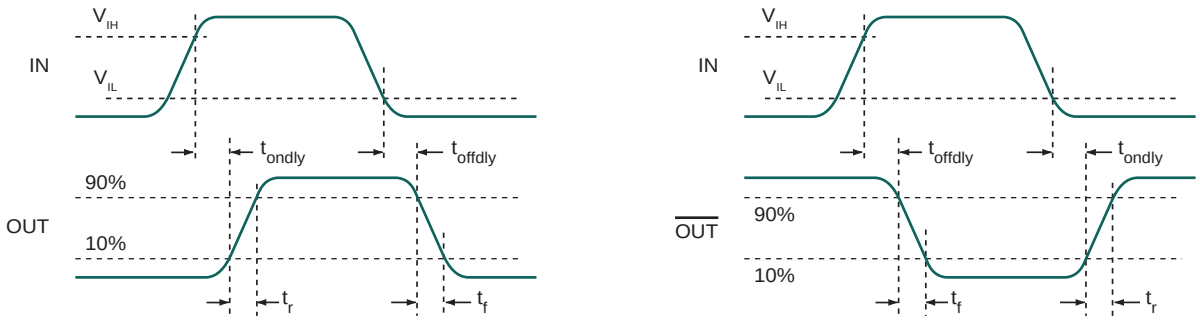
Parameter	Conditions	Symbol	Minimum	Maximum	Units
Input Voltage, High	4.5V ≤ V_{CC} ≤ 18V	V_{IH}	3.3	-	V
Input Voltage, Low	4.5V ≤ V_{CC} ≤ 18V	V_{IL}	-	0.65	
Input Current	0V ≤ V_{IN} ≤ V_{CC}	I_{IN}	-	±10	µA
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	V
Output Voltage, Low	-	V_{OL}	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	2	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	1.5	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	±1	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	40	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	30	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	75	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	75	
Enable to Output-High Delay Time	IXDD609SI only, V_{CC}=18V	t_{ENOH}	-	75	
Disable to High Impedance State Delay Time	IXDD609SI only, V_{CC}=18V	t_{DOLD}	-	75	
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	2.5	mA
	V_{CC}=18V, V_{IN}=0V		-	150	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	150	

1.7 Thermal Characteristics

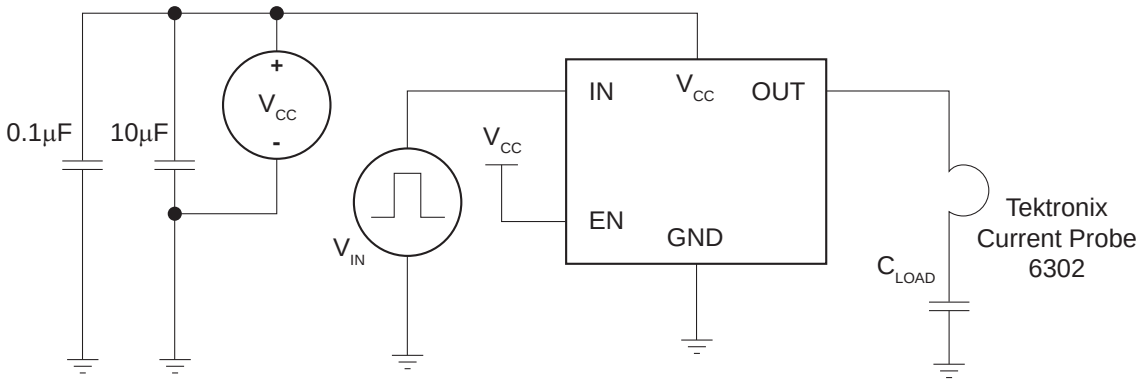
Package	Parameter	Symbol	Rating	Units
SI (8-Pin Power SOIC)	Thermal Resistance, Junction-to-Ambient	θ_{JA}	85	°C/W
	Thermal Resistance, Junction-to-Case	θ_{JC}	10	

2 IXD_609SI Performance

2.1 Timing Diagrams

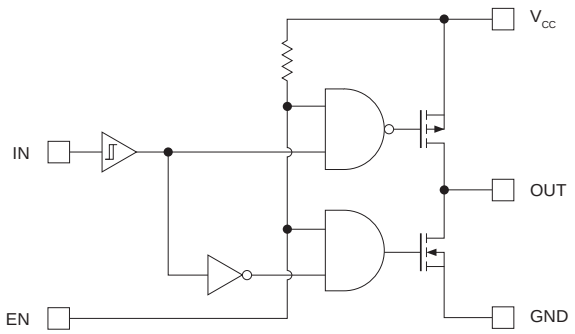


2.2 Characteristics Test Diagram



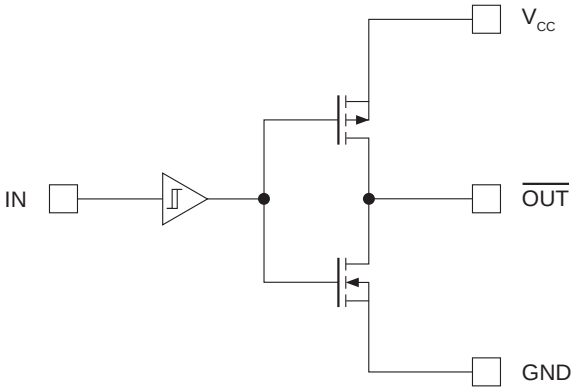
3 Block Diagrams & Truth Tables

3.1 IXDD609SI



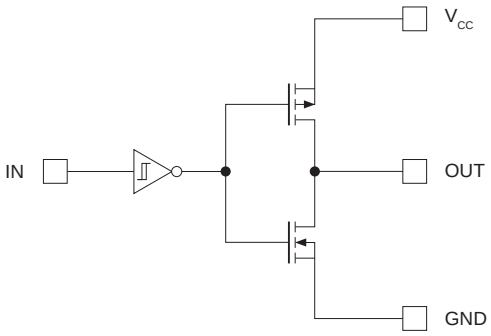
IN	EN	OUT
0	1 or open	0
1	1 or open	1
x	0	Z

3.2 IXDI609SI



IN	$\overline{OUT}$
0	1
1	0

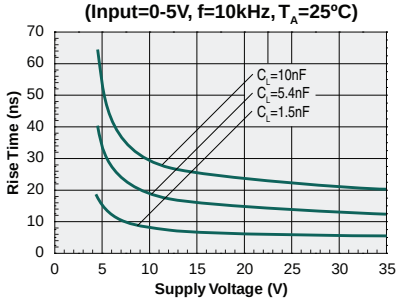
3.3 IXDN609SI



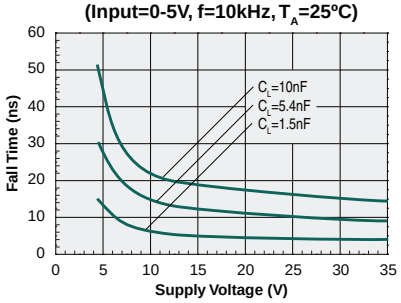
IN	OUT
0	0
1	1

4 Typical Performance Characteristics

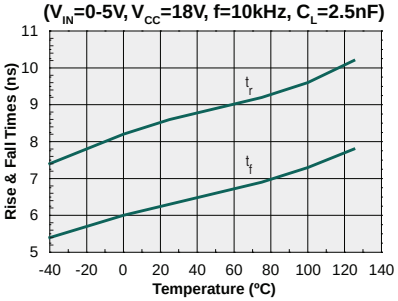
Rise Time vs. Supply Voltage (Input=0-5V, f=10kHz, T_A=25ºC)



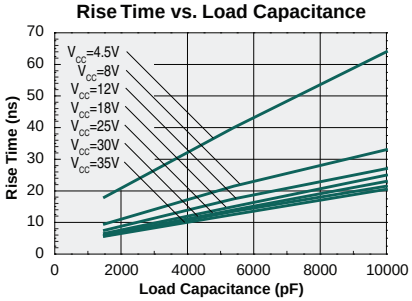
Fall Time vs. Supply Voltage (Input=0-5V, f=10kHz, T_A=25ºC)



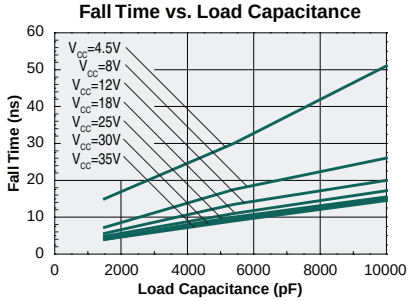
Rise and Fall Times vs. Temperature (V_{IN}=0-5V, V_{CC}=18V, f=10kHz, C_L=2.5nF)



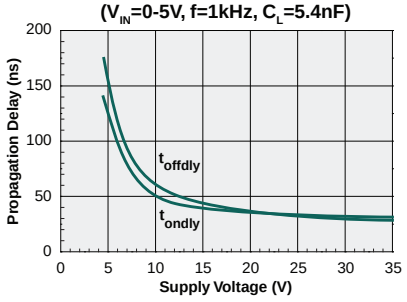
Rise Time vs. Load Capacitance



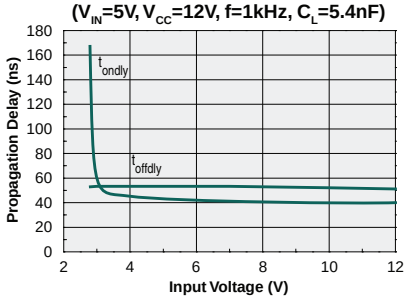
Fall Time vs. Load Capacitance



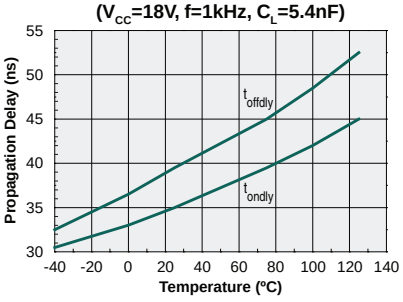
Propagation Delay vs. Supply Voltage (V_{IN}=0-5V, f=1kHz, C_L=5.4nF)



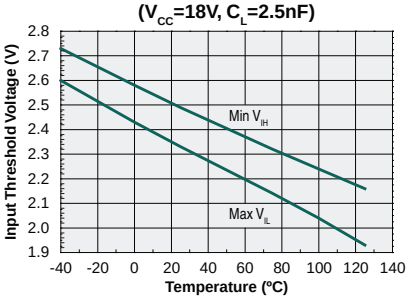
Propagation Delay vs. Input Voltage (V_{IN}=5V, V_{CC}=12V, f=1kHz, C_L=5.4nF)



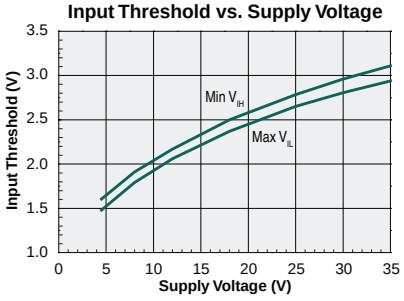
Propagation Delay vs. Temperature (V_{CC}=18V, f=1kHz, C_L=5.4nF)



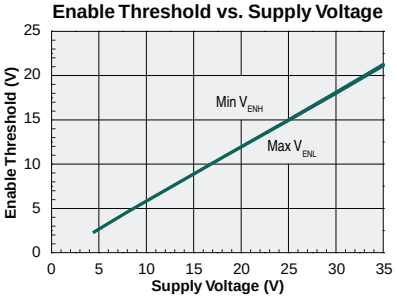
Input Threshold Voltage vs. Temperature (V_{CC}=18V, C_L=2.5nF)



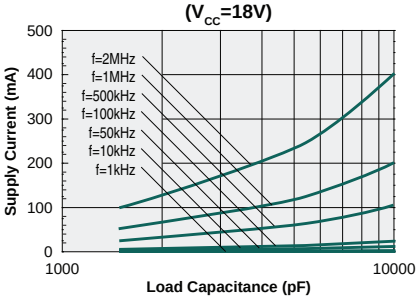
Input Threshold vs. Supply Voltage



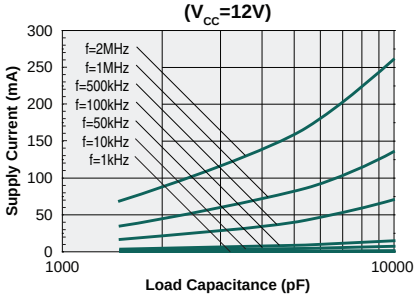
Enable Threshold vs. Supply Voltage



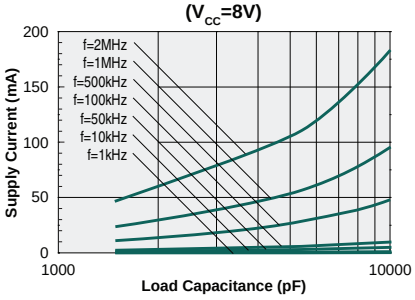
Supply Current vs. Load Capacitance (V_{CC}=18V)



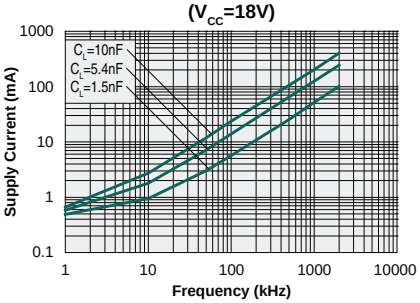
Supply Current vs. Load Capacitance (V_{CC}=12V)



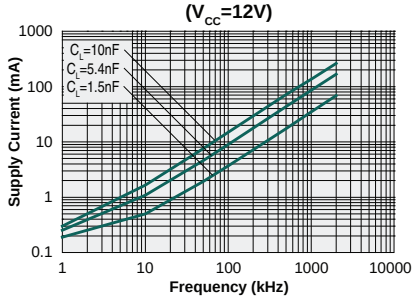
Supply Current vs. Load Capacitance (V_{CC}=8V)



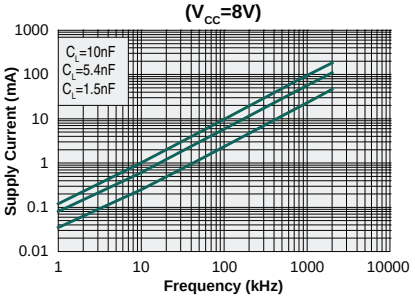
Supply Current vs. Frequency (V_{CC}=18V)



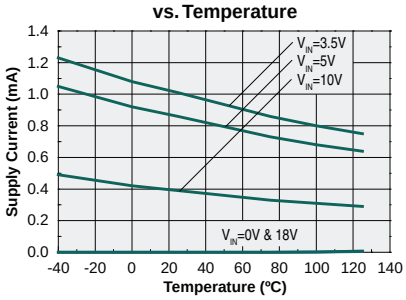
Supply Current vs. Frequency (V_{CC}=12V)



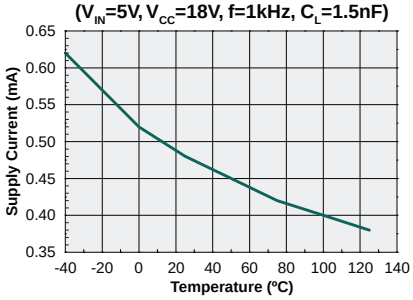
Supply Current vs. Frequency (V_{CC}=8V)



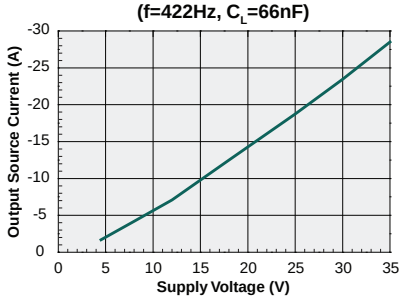
Quiescent Supply Current vs. Temperature



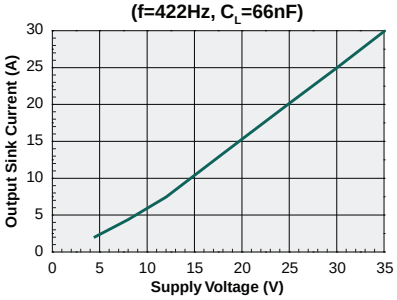
Dynamic Supply Current vs. Temperature (V_{IN}=5V, V_{CC}=18V, f=1kHz, C_L=1.5nF)



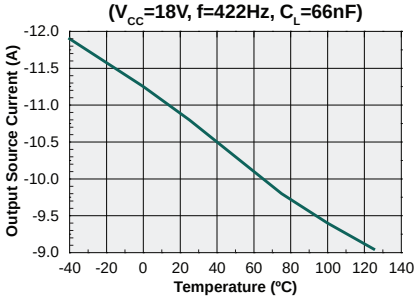
Output Source Current vs. Supply Voltage (f=422Hz, C_L=66nF)



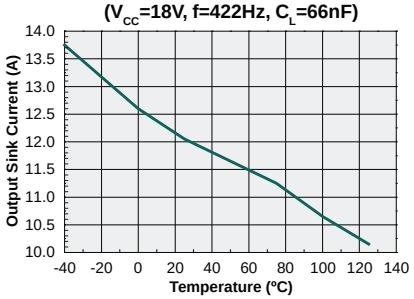
Output Sink Current vs. Supply Voltage (f=422Hz, C_L=66nF)



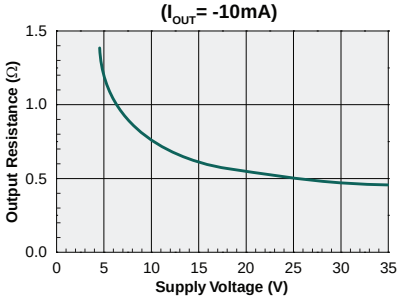
Output Source Current vs. Temperature (V_{CC}=18V, f=422Hz, C_L=66nF)



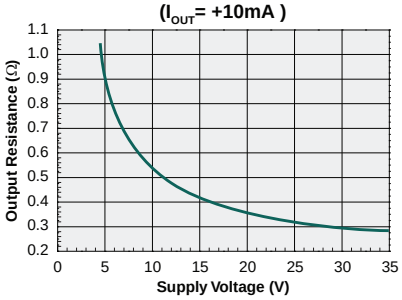
Output Sink Current vs. Temperature (V_{CC}=18V, f=422Hz, C_L=66nF)



High State Output Resistance vs. Supply Voltage (I_{OUT}= -10mA)



Low State Output Resistance vs. Supply Voltage (I_{OUT}= +10mA)



5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IXD_609SI	MSL 1

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

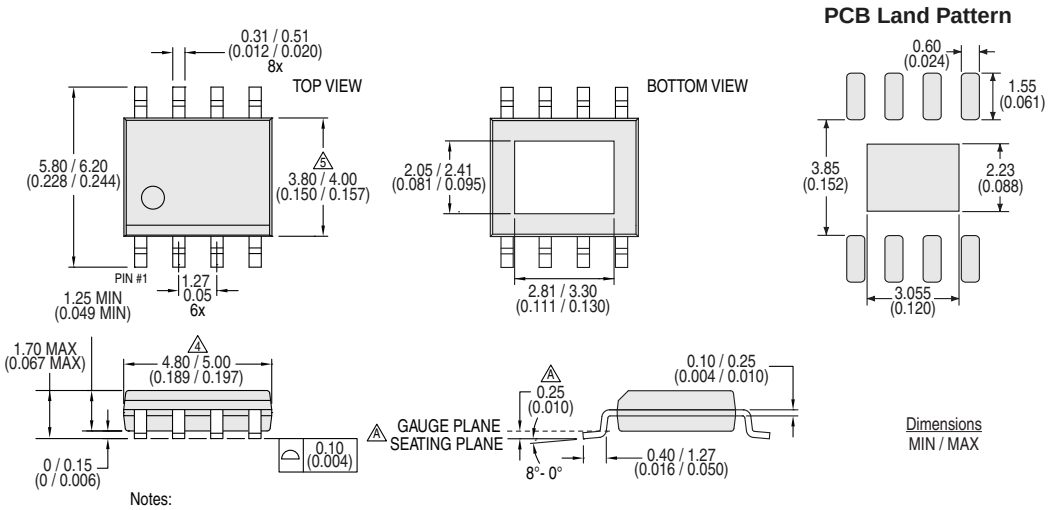
Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IXD_609SI	260°C	30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.Mechanica dimensions.

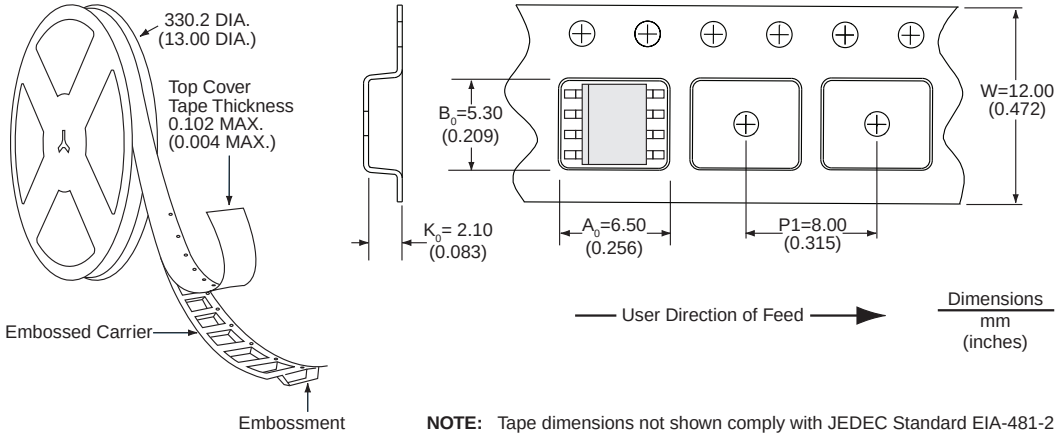
5.4.1 SI Package (8-Pin Power SOIC with Exposed Metal Back)



Notes:

1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
4. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
5. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. The exposed metal pad on the back of the package should be connected to GND. It is not suitable for carrying current.
7. Lead thickness includes plating.

5.4.2 Tape & Reel Information for SI Package



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

For additional information please visit our website at: www.ixysic.com

Specification: DS-IXD_609SI-R02

10/25/2017

The information below supercedes any previously presented material.

For additional information please visit our website at: https://www.littelfuse.com

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