

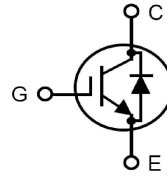
High Voltage, BiMOSFET™ Monolithic Bipolar MOS Transistor

IXBF42N300

$$V_{CES} = 3000V$$

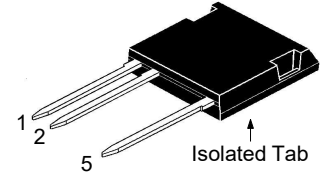
$$I_{C110} = 24A$$

$$V_{CE(sat)} \leq 3.0V$$



(Electrically Isolated Tab)

ISOPLUS i4-Pak™



1 = Gate
2 = Emitter

5 = Collector

| Symbol | Test Conditions | Maximum Ratings | |
|------------------------------------|--|-------------------|------------|
| V_{CES} | $T_C = 25^\circ C$ to $150^\circ C$ | 3000 | V |
| V_{CGR} | $T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$ | 3000 | V |
| V_{GES} | Continuous | ± 25 | V |
| V_{GEM} | Transient | ± 35 | V |
| I_{C25} | $T_C = 25^\circ C$ | 60 | A |
| I_{C110} | $T_C = 110^\circ C$ | 24 | A |
| I_{CM} | $T_C = 25^\circ C$, 1ms | 400 | A |
| SSOA (RBSOA) | $V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 20\Omega$ | $I_{CM} = 84$ | A |
| | Clamped Inductive Load | 1500 | V |
| T_{SC} (SCSOA) | $V_{GE} = 15V$, $T_J = 125^\circ C$, $R_G = 82\Omega$, $V_{CE} = 1500V$, Non-Repetitive | 10 | μs |
| P_C | $T_C = 25^\circ C$ | 240 | W |
| T_J | | -55 ... +150 | $^\circ C$ |
| T_{JM} | | 150 | $^\circ C$ |
| T_{stg} | | -55 ... +150 | $^\circ C$ |
| T_L | Maximum Lead Temperature for Soldering 1.6 mm (0.062 in.) from Case for 10s | 300 | $^\circ C$ |
| F_C | Mounting Force | 20..120 / 4.5..27 | N/lb |
| V_{ISOL} | 50/60Hz, 1 Minute | 3000 | V~ |
| Weight | | 5 | g |

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 3000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage
- FBSOA Rated
- SCSOA Rated

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Laser Generators
- Capacitor Discharge Circuits
- AC Switches
- Protection Circuits

| Symbol | Test Conditions ($T_J = 25^\circ C$ Unless Otherwise Specified) | Characteristic Values | | |
|---------------|---|-----------------------|------|-----------------------|
| | | Min. | Typ. | Max. |
| BV_{CES} | $I_C = 1mA$, $V_{GE} = 0V$ | 3000 | | V |
| $V_{GE(th)}$ | $I_C = 1mA$, $V_{CE} = V_{GE}$ | 3.0 | | 5.0 V |
| I_{CES} | $V_{CE} = 0.8 \cdot V_{CES}$, $V_{GE} = 0V$ Note 2, $T_J = 125^\circ C$ | | 250 | 50 μA μA |
| I_{GES} | $V_{CE} = 0V$, $V_{GE} = \pm 25V$ | | | ± 200 nA |
| $V_{CE(sat)}$ | $I_C = 42A$, $V_{GE} = 15V$, Note 1 $T_J = 125^\circ C$ | | 2.5 | 3.0 V |
| | | | 3.1 | V |

| Symbol Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified) | | Characteristic Values | | |
|--|--|-----------------------|------|-------------------------|
| | | Min. | Typ. | Max. |
| g_{fs} | $I_C = 42\text{A}, V_{CE} = 10\text{V}$, Note 1 | 28 | 45 | S |
| C_{ies} | $V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$ | | 4780 | pF |
| C_{oes} | | | 170 | pF |
| C_{res} | | | 56 | pF |
| R_{Gi} | Gate Input Resistance | | 3.0 | Ω |
| Q_g | $I_C = 42\text{A}, V_{GE} = 15\text{V}, V_{CE} = 1000\text{V}$ | | 200 | nC |
| Q_{ge} | | | 28 | nC |
| Q_{gc} | | | 75 | nC |
| $t_{d(on)}$ | Resistive Switching Times, $T_J = 25^\circ\text{C}$ $I_C = 42\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1500\text{V}, R_G = 20\Omega$ | | 72 | ns |
| t_r | | | 330 | ns |
| $t_{d(off)}$ | | | 445 | ns |
| t_f | | | 610 | ns |
| $t_{d(on)}$ | Resistive Switching Times, $T_J = 125^\circ\text{C}$ $I_C = 42\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1500\text{V}, R_G = 20\Omega$ | | 72 | ns |
| t_r | | | 580 | ns |
| $t_{d(off)}$ | | | 460 | ns |
| t_f | | | 490 | ns |
| R_{thJC} | | | | 0.52 $^\circ\text{C/W}$ |
| R_{thCS} | | 0.15 | | $^\circ\text{C/W}$ |

Reverse Diode

| Symbol Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified) | | Characteristic Values | | |
|--|---|-----------------------|------|---------------|
| | | Min. | Typ. | Max. |
| V_F | $I_F = 42\text{A}, V_{GE} = 0\text{V}$, Note 1 | | | 2.5 V |
| t_{rr} | $I_F = 21\text{A}, V_{GE} = 0\text{V}, -di_F/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GE} = 0\text{V}$ | | 1.7 | μs |
| I_{RM} | | | 43 | A |

Notes:

1. Pulse test, $t < 300\mu\text{s}$, duty cycle, $d < 2\%$.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

Additional provisions for lead-to-lead isolation are required at $V_{CE} > 1250\text{V}$.

Littelfuse reserves the right to change limits, test conditions and dimensions.

| | | | | | | | | | | |
|---|-----------|-----------|-----------|-----------|--------------|-------------|-------------|--------------|--------------|-------------|
| LFMOSFETs and IGBTs are covered by one or more of the following U.S. patents: | 4,835,592 | 4,931,844 | 5,049,961 | 5,237,481 | 6,162,665 | 6,404,065B1 | 6,683,344 | 6,727,585 | 7,005,734 B2 | 7,157,338B2 |
| | 4,860,072 | 5,017,508 | 5,063,307 | 5,381,025 | 6,259,123B1 | 6,534,343 | 6,710,405B2 | 6,759,692 | 7,063,975B2 | |
| | 4,881,106 | 5,034,796 | 5,187,117 | 5,486,715 | 6,306,728 B1 | 6,583,505 | 6,710,463 | 6,771,478 B2 | 7,071,537 | |

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

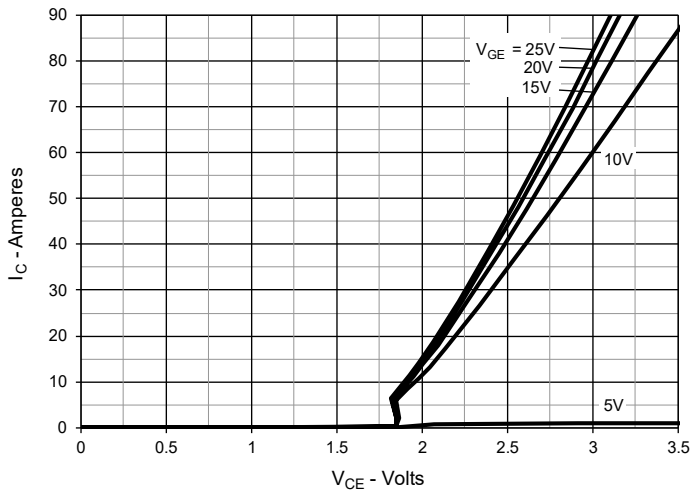


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

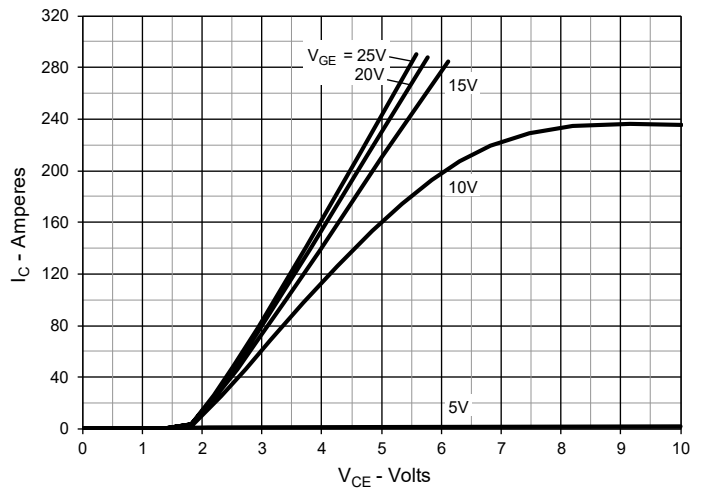


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

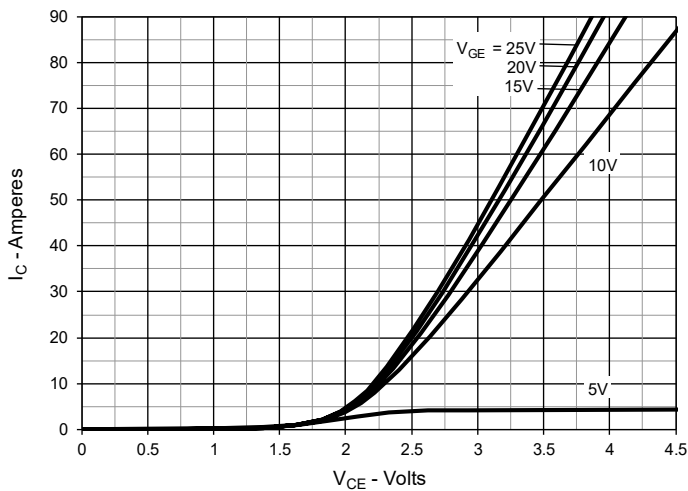


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

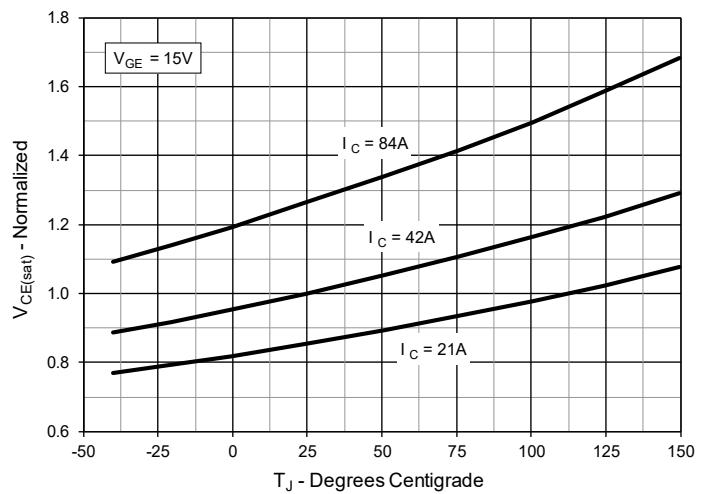


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

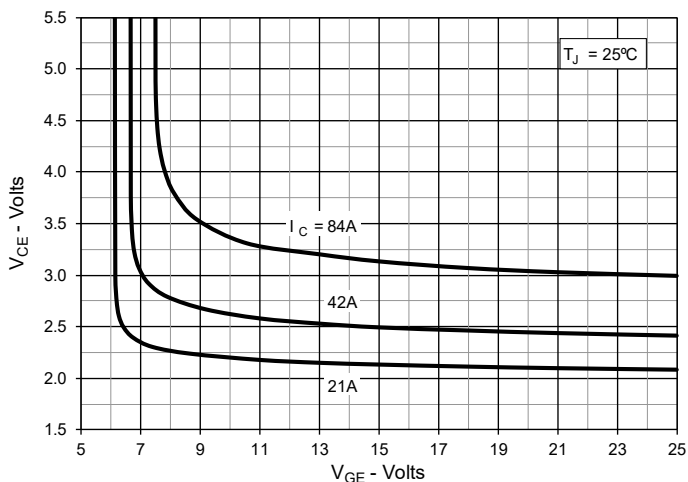


Fig. 6. Input Admittance

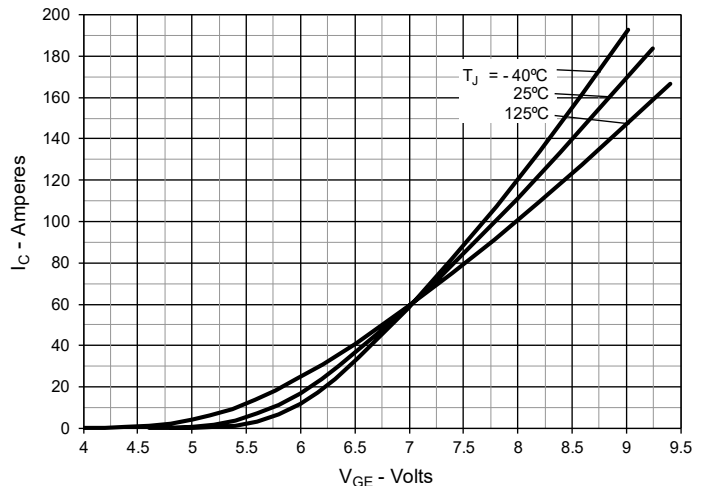


Fig. 7. Transconductance

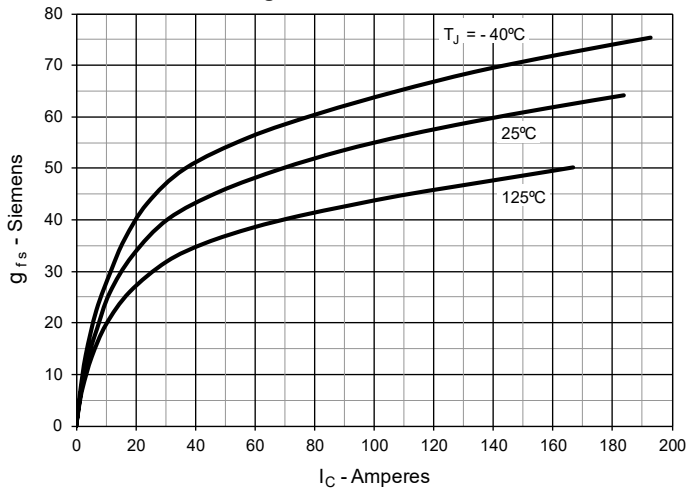


Fig. 8. Forward Voltage Drop of Intrinsic Diode

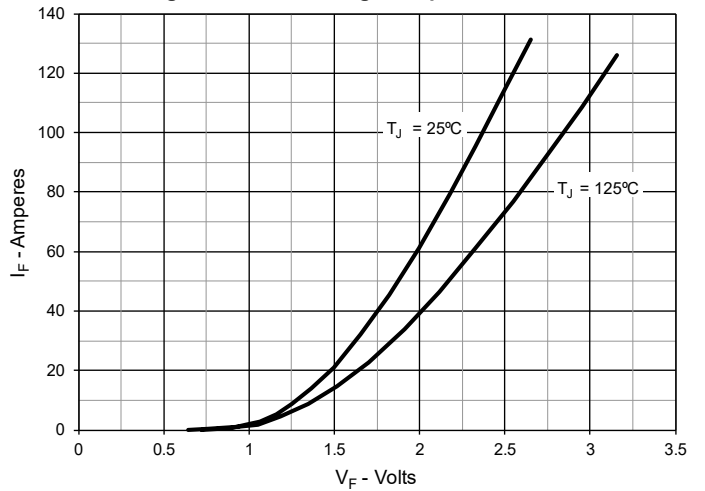


Fig. 9. Gate Charge

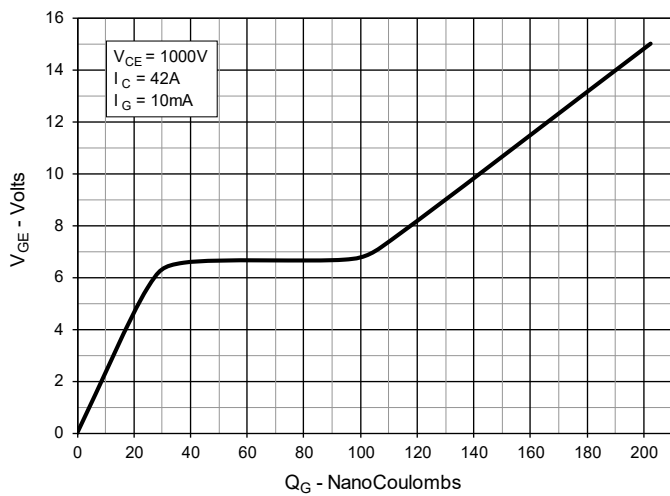


Fig. 10. Capacitance

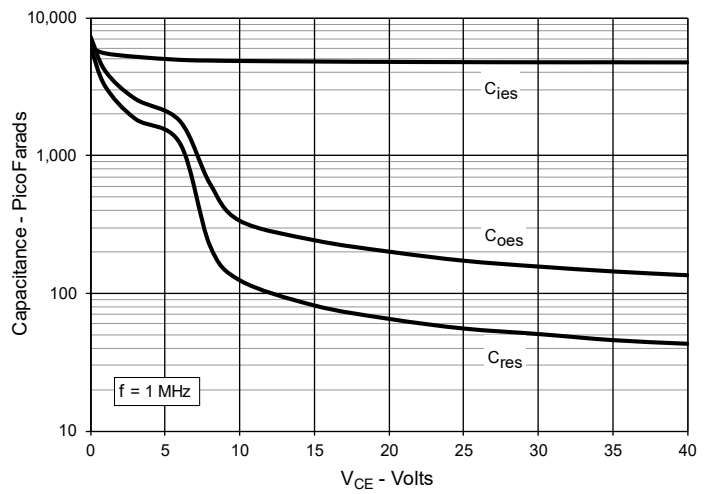


Fig. 11. Reverse-Bias Safe Operating Area

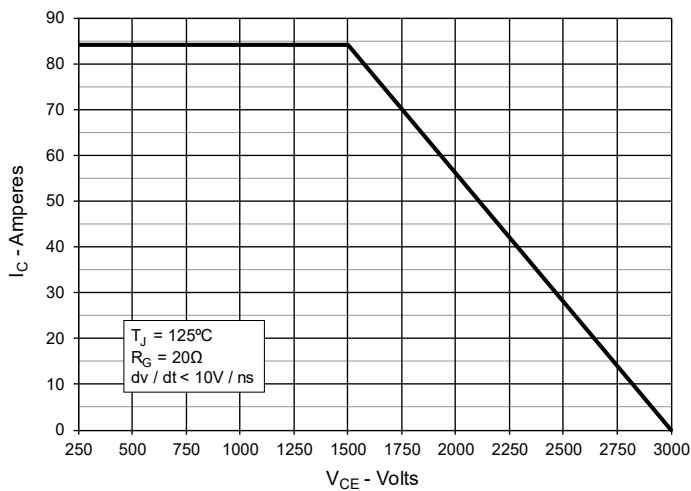


Fig. 12. Maximum Transient Thermal Impedance

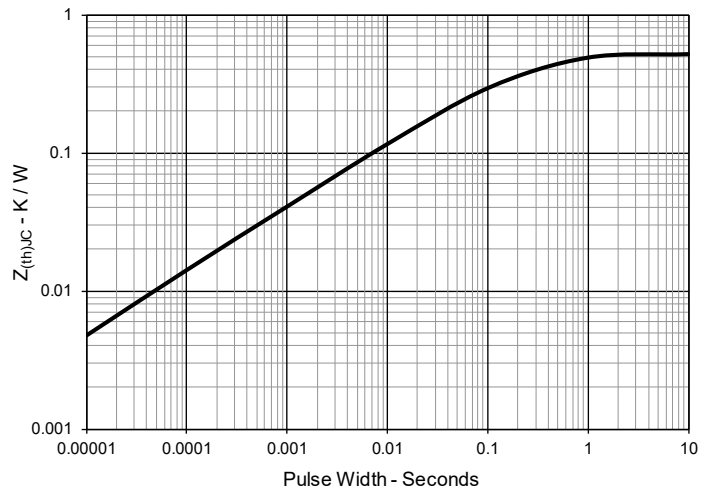


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

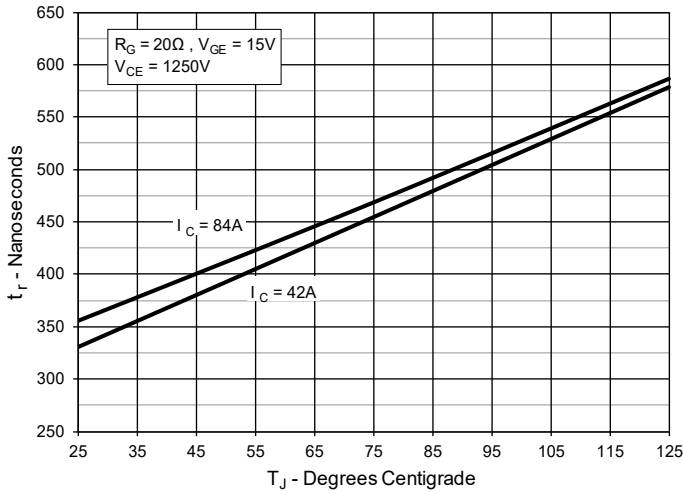


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

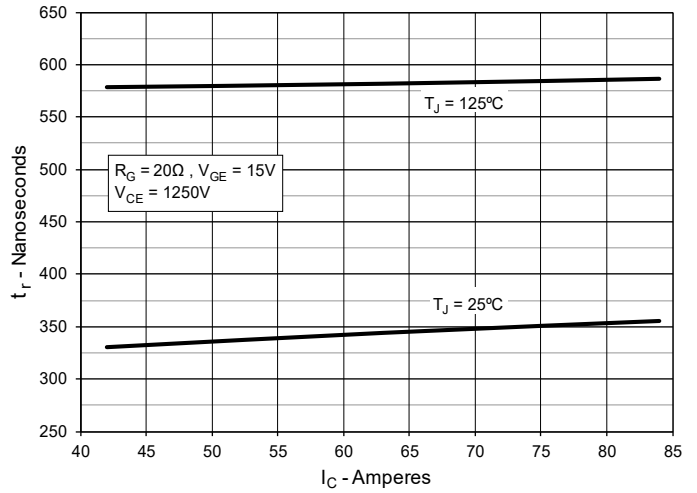


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

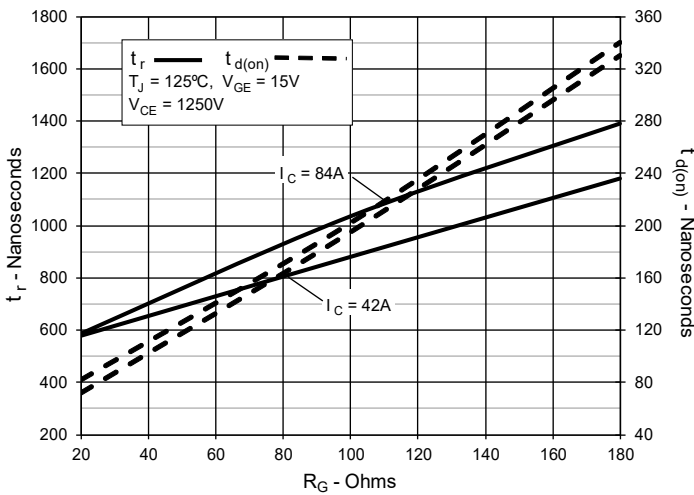


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

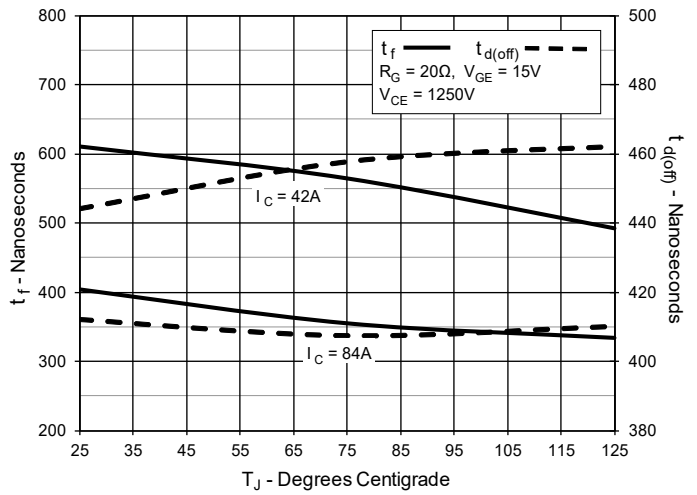


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

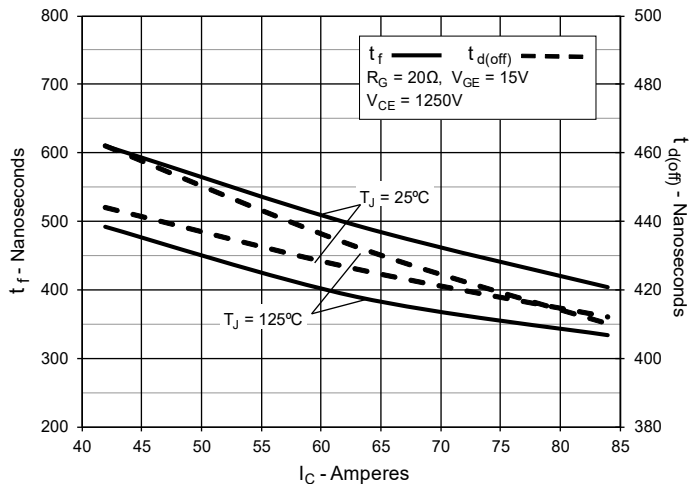


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

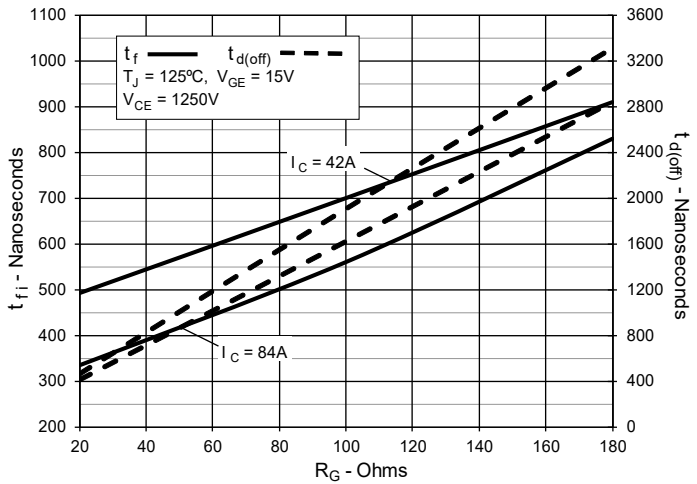


Fig. 19. Forward-Bias Safe Operating Area @ $T_C = 25^\circ\text{C}$

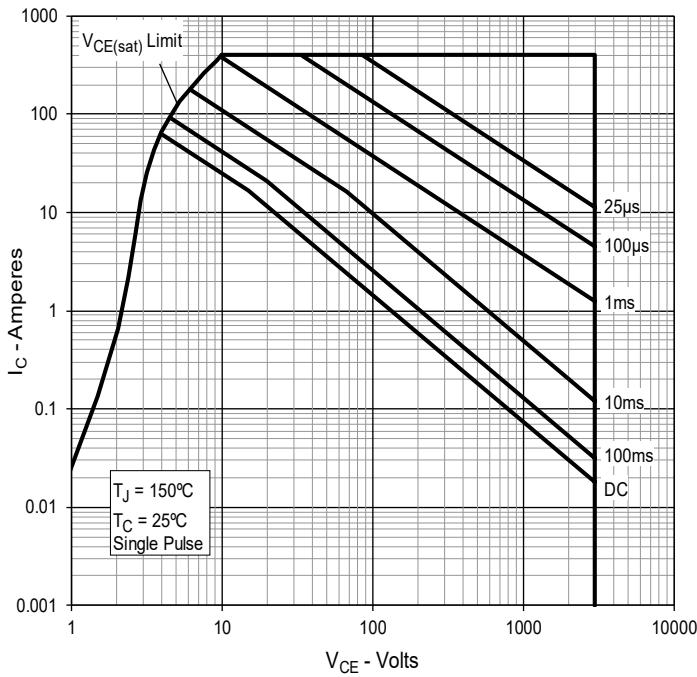
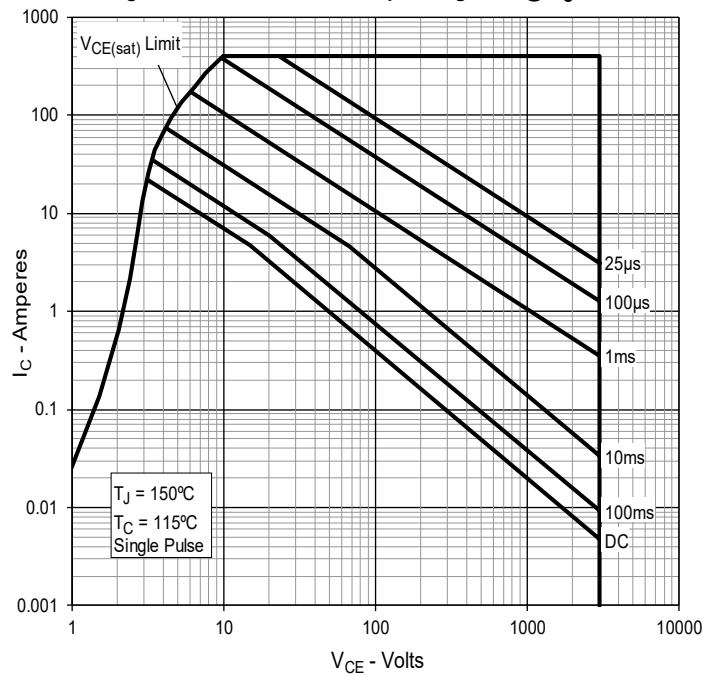
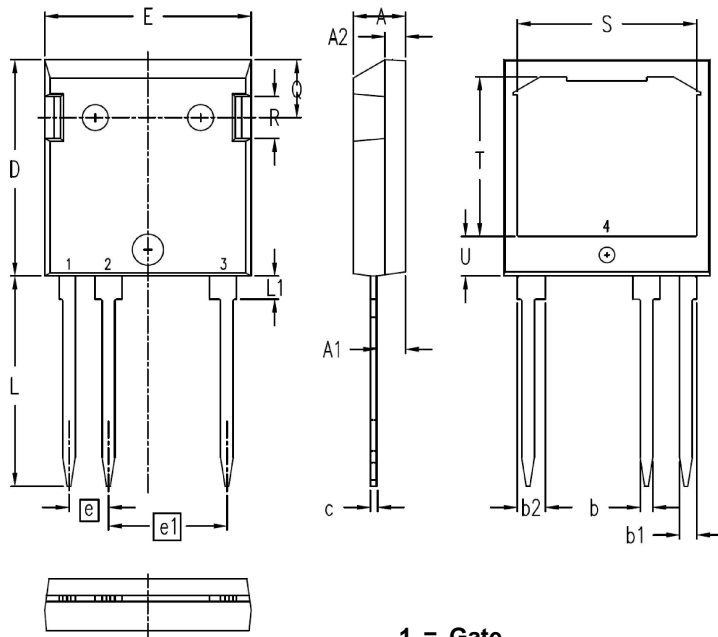


Fig. 20. Forward-Bias Safe Operating Area @ $T_C = 115^\circ\text{C}$



ISOPLUS i4-Pak Outline



1 = Gate
2 = Emitter
3,4 = Colector

| SYM | INCHES | | MILLIMETERS | |
|-----|----------|------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | .193 | .201 | 4.90 | 5.10 |
| A1 | .106 | .114 | 2.70 | 2.90 |
| A2 | .075 | .083 | 1.90 | 2.10 |
| b | .047 | .055 | 1.20 | 1.40 |
| b1 | .061 | .069 | 1.55 | 1.75 |
| b2 | .087 | .094 | 2.20 | 2.40 |
| c | .020 | .029 | 0.51 | 0.74 |
| D | .819 | .846 | 20.80 | 21.50 |
| E | .768 | .799 | 19.50 | 20.30 |
| e | .150 BSC | | 3.81 BSC | |
| e1 | .450 BSC | | 11.43 BSC | |
| L | .780 | .838 | 19.80 | 21.30 |
| L1 | .083 | .094 | 2.10 | 2.40 |
| Q | .213 | .236 | 5.40 | 6.00 |
| R | .157 | .169 | 4.00 | 4.30 |
| S | .673 | .685 | 17.10 | 17.40 |
| T | .602 | .614 | 15.30 | 15.60 |
| U | .142 | .154 | 3.60 | 3.90 |