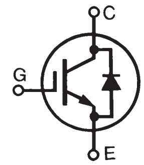
Preliminary Technical Information

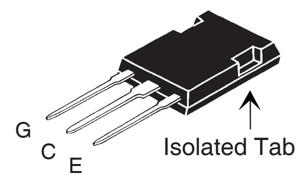
High Voltage, High Gain BIMOSFET™ Monolithic Bipolar MOS Transistor

IXBR42N170

V_{CES} = 1700V
I_{C90} = 32A
$V_{CE(sat)} \leq$ 2.9V



ISOPLUS247™
E153432



G = Gate
C = Collector
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	1700	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1700	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	57	A
I_{C90}	T_C = 90°C	32	A
I_{CM}	T_C = 25°C, 1ms	300	A
SSOA	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 10Ω	I_{CM} = 100	A
(RBSOA)	Clamped inductive load	$V_{CES} \leq$ 1350	V
P_C	T_C = 25°C	200	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from case for 10s	300	°C
T_{SOLD}	Plastic body for 10 seconds	260	°C
F_C	Mounting force	20..120 / 4.5..27	Nm/lb.in.
V_{ISOL}	50/60 Hz, RMS t = 1min	2500	V~
	$I_{ISOL} \leq$ 1mA t = 1s	3000	V~
Weight		5	g

Features

- Silicon chip on Direct-Copper Bond (DCB) substrate
- Isolated mounting surface
- 2500V electrical isolation

Advantages

- Low gate drive requirement
- High power density

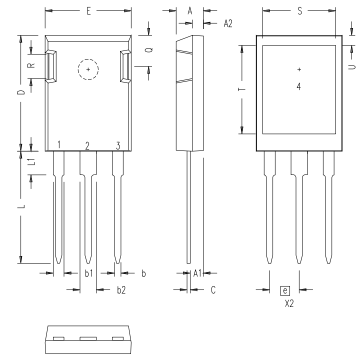
Applications:

- Switched-mode and resonant-mode power supplies
- Uninterruptible power supplies (UPS)
- Laser generator
- Capacitor discharge circuit
- AC switches

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)		Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V		1700			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}		2.5		5.5	V
I_{CES}	V_{CE} = 0.8 • V_{CES}				50	μA
	V_{GE} = 0V	T_J = 125°C			1.5	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 20V				±100	nA
$V_{CE(sat)}$	I_C = 42A, V_{GE} = 15V, Note 1				2.9	V
		T_J = 125°C		2.7		V

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Min.	Typ.	Max.	
g_{fS}	I_C = 42A, V_{CE} = 10V, Note 1	24	32		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		3990		pF
C_{oes}			225		pF
C_{res}			70		pF
Q_g	I_C = 42A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		188		nC
Q_{ge}			29		nC
Q_{gc}			76		nC
$t_{d(on)}$	**Resistive Switching times, T_J = 25°C**		37		ns
t_r	I_C = 42A, V_{GE} = 15V		139		ns
$t_{d(off)}$	V_{CE} = 850V, R_G = 10Ω		340		ns
t_f			665		ns
$t_{d(on)}$	**Resistive Switching times, T_J = 125°C**		36		ns
t_r	I_C = 42A, V_{GE} = 15V		188		ns
$t_{d(off)}$	V_{CE} = 850V, R_G = 10Ω		330		ns
t_f			740		ns
R_{thJC}				0.62	°C/W
R_{thCS}			0.15		°C/W

ISOPLUS247 (IXBR) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Reverse Diode

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Min.	Typ.	Max.	
V_F	I_F = 42A, V_{GE} = 0V			2.8	V
t_{rr}	I_F = 21A, V_{GE} = 0V, -di_F/dt = 100A/μs		1.32		μs
I_{RM}	V_R = 100V		36		A

Note 1: Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ 25ºC

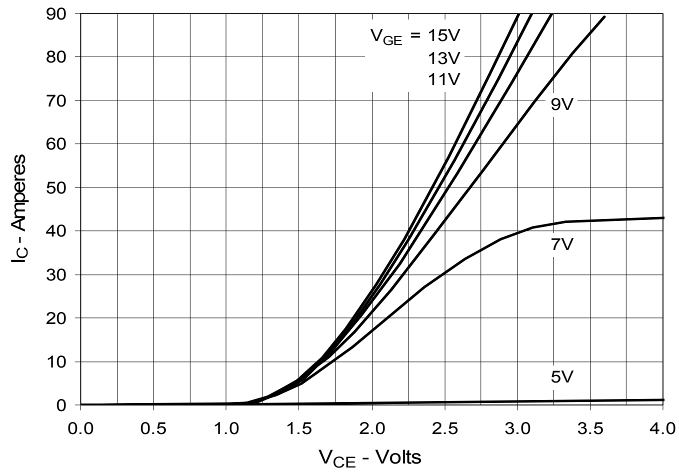


Fig. 2. Extended Output Characteristics @ 25ºC

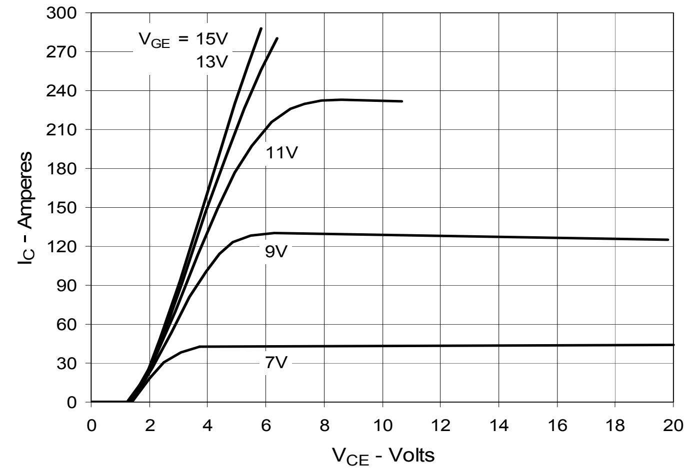


Fig. 3. Output Characteristics @ 125ºC

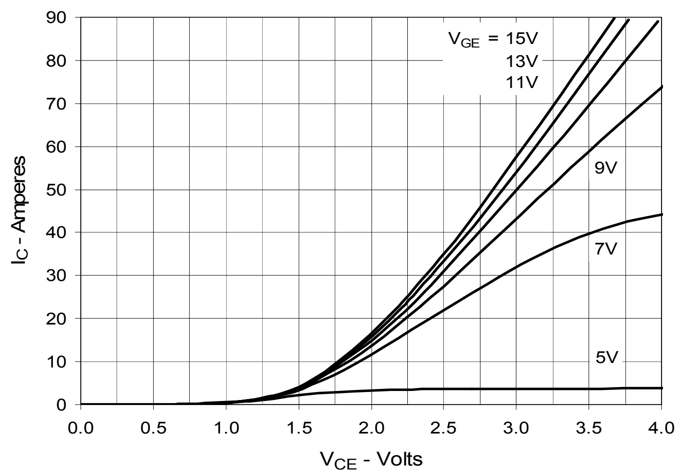


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

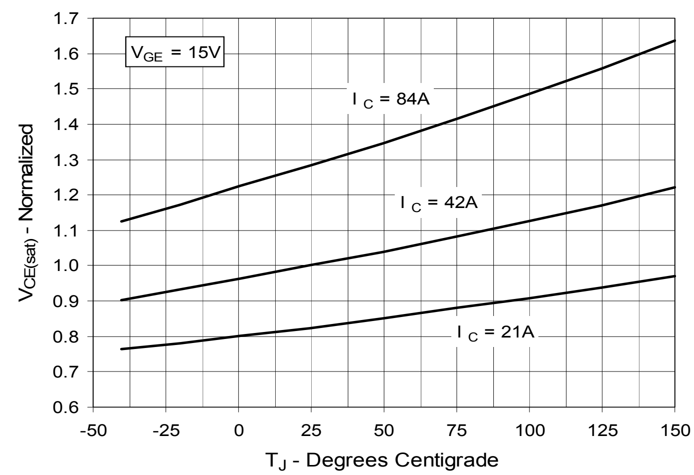


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

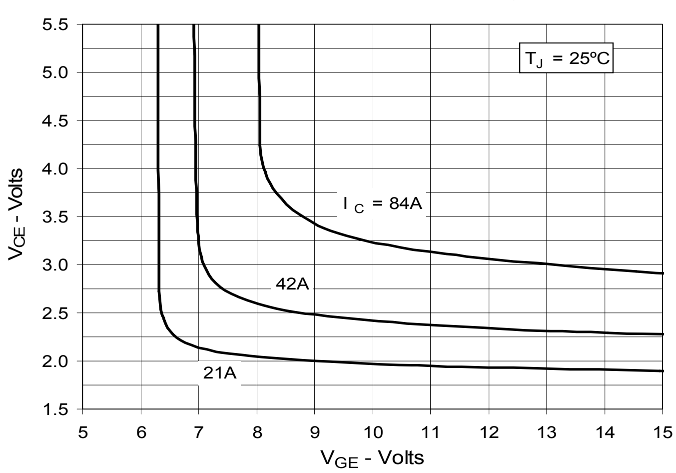


Fig. 6. Input Admittance

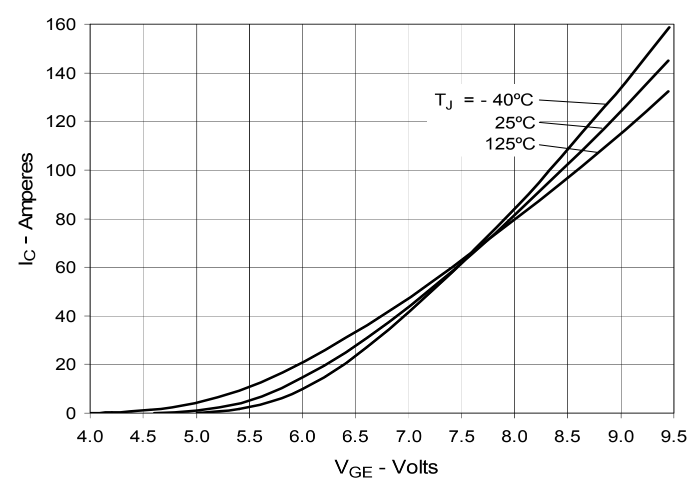


Fig. 7. Transconductance

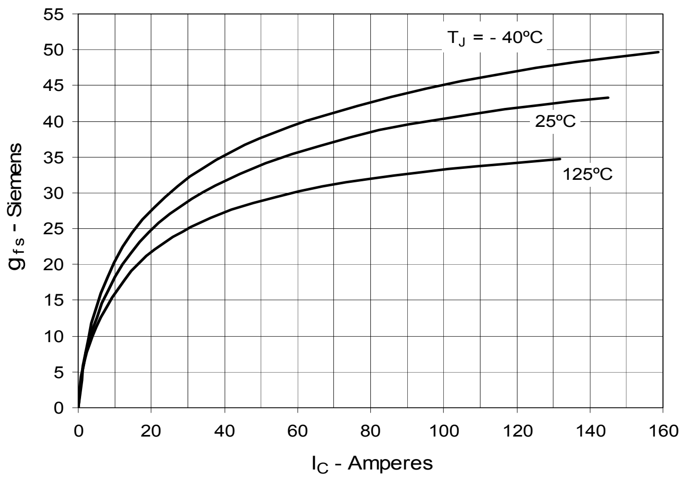


Fig. 8. Forward Voltage Drop of Intrinsic Diode

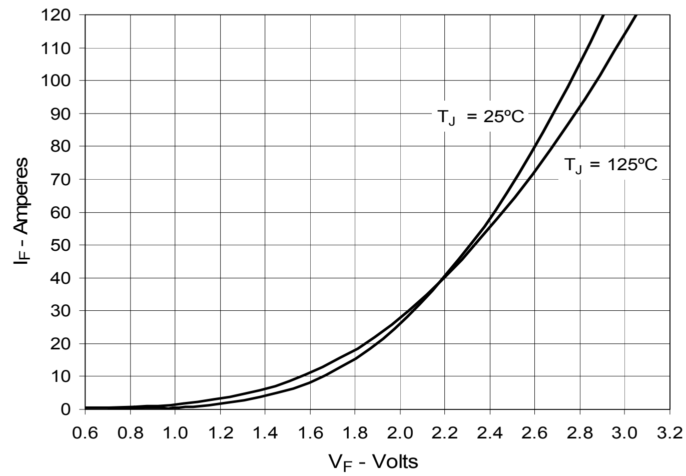


Fig. 9. Gate Charge

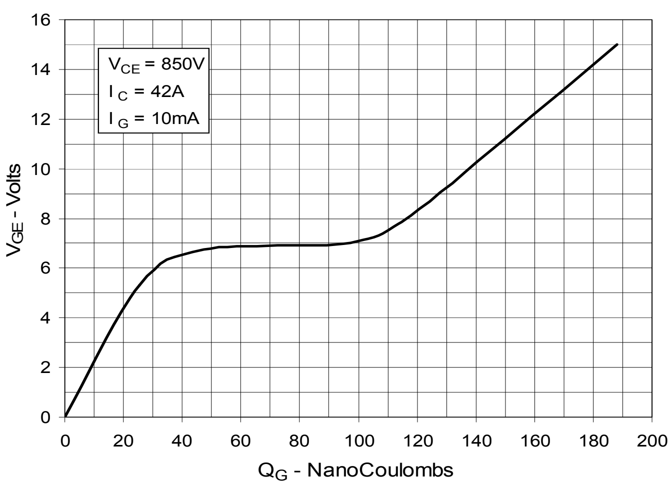


Fig. 10. Capacitance

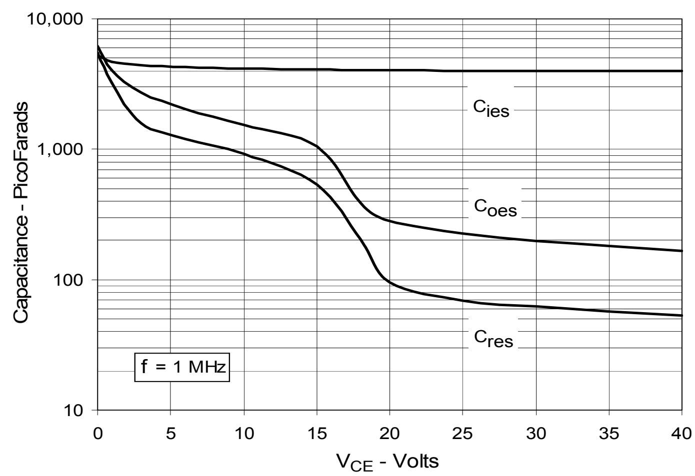


Fig. 11. Reverse-Bias Safe Operating Area

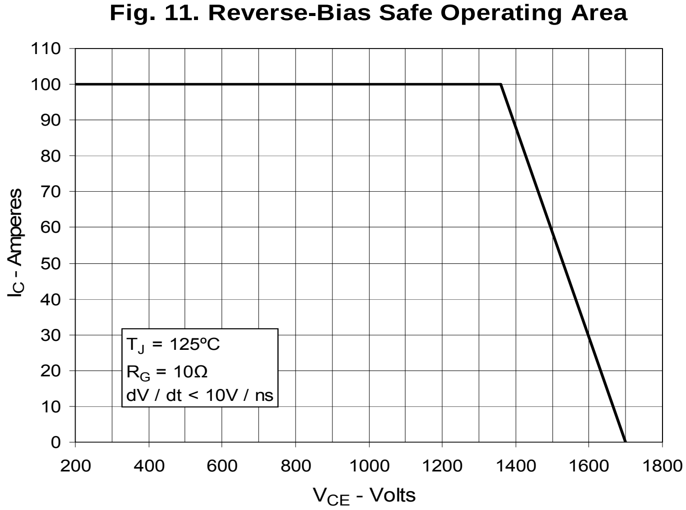


Fig. 12. Maximum Transient Thermal Impedance

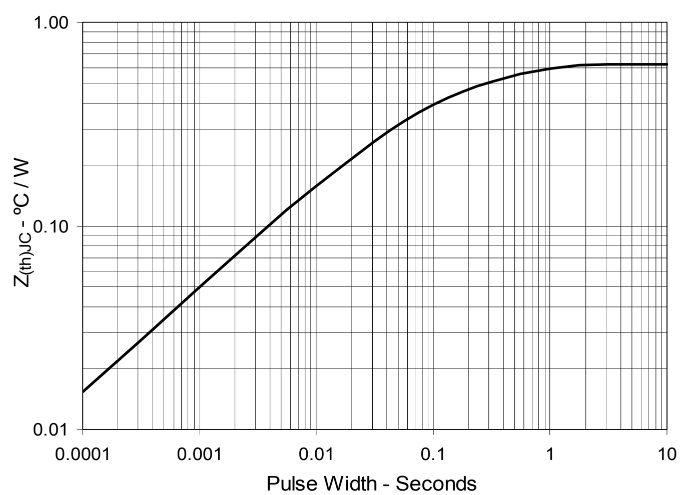


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

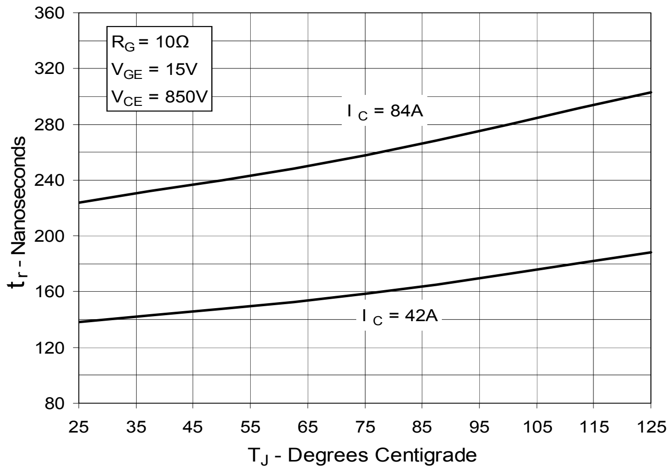


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

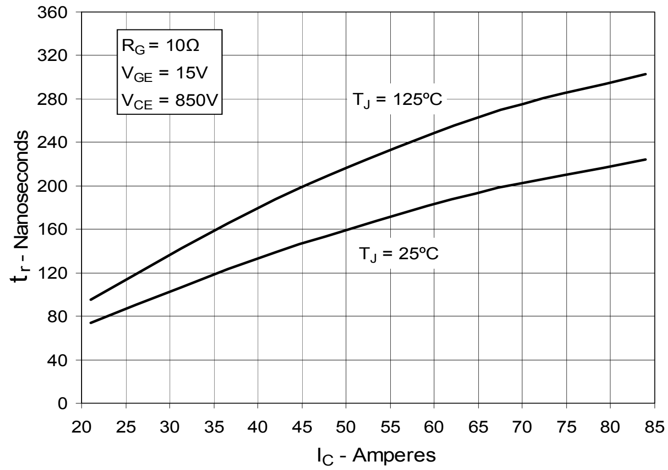


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

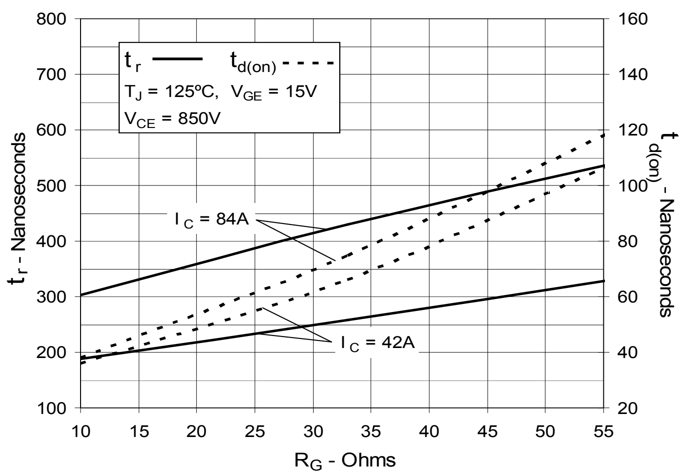


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

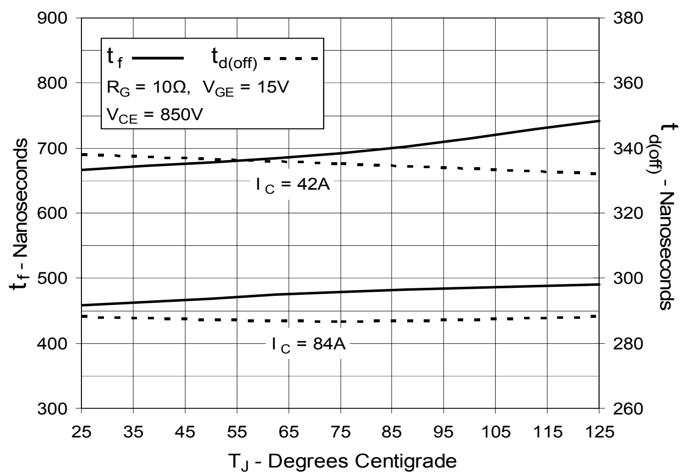


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

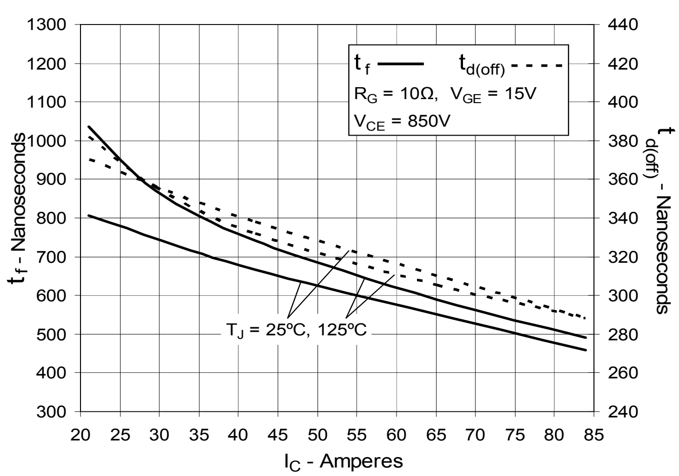


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance