IXYS

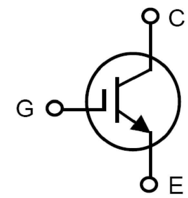
Not For New Designs

High Voltage IGBT
For Capacitor Discharge Applications

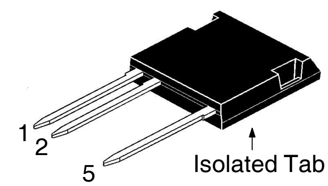
IXGF30N400

V_{CES} = 4000V
I_{C25} = 30A
$V_{CE(sat)}$ ≤ 3.1V

(Electrically Isolated Tab)



ISOPLUS i4-Pak™



1 = Gate   5 = Collector
2 = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	4000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	30	A
I_{C110}	T_C = 110°C	15	A
I_{CM}	T_C = 25°C, V_{GE} = 20V, 1ms	360	A
SSOA	V_{GE}= 20V, T_{VJ} = 125°C, R_G = 2Ω	I_{CM} = 300	A
(RBSOA)	Clamped Inductive Load	$V_{CE} \leq 0.8 \cdot V_{CES}$	
P_C	T_C = 25°C	160	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
F_C	Mounting Force	20..120 / 4.5..27	Nm/lb.in.
V_{ISOL}	50/60Hz, 1 minute	4000	V~
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	4000			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			50	μA
	Note 2, T_J = 100°C			3	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±200	nA
$V_{CE(sat)}$	I_C = 30A, V_{GE} = 15V, Note 1			3.1	V
	I_C = 90A			5.2	V

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V Electrical Isolation
- High Peak Current Capability
- Low Saturation Voltage
- Molding Epoxies Meet UL 94 V-0 Flammability Classification

Advantages

- High Power Density
- Easy to Mount

Applications

- Capacitor Discharge
- Pulser Circuits

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Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 30A, V_{CE} = 10V, Note 1	14	23		S
$I_{C(ON)}$	V_{GE} = 15V, V_{CE} = 20V, Note 1		360		A
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		3040		pF
C_{oes}			95		pF
C_{res}			30		pF
Q_g	I_C = 30A, V_{GE} = 15V, V_{CE} = 600V		135		nC
Q_{ge}			22		nC
Q_{gc}			50		nC
$t_{d(on)}$	**Resistive Switching Times** I_C = 30A, V_{GE} = 15V, V_{CE} = 1250V, R_G = 2Ω		55		ns
t_r			146		ns
$t_{d(off)}$			210		ns
t_f			514		ns
R_{thJC}				0.78	°C/W
R_{thCS}			0.15		°C/W
R_{thJA}			30		°C/W

Notes:

1. Pulse test, t < 300μs, duty cycle, d < 2%.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

Fig. 1. Output Characteristics @ T_J = 25ºC

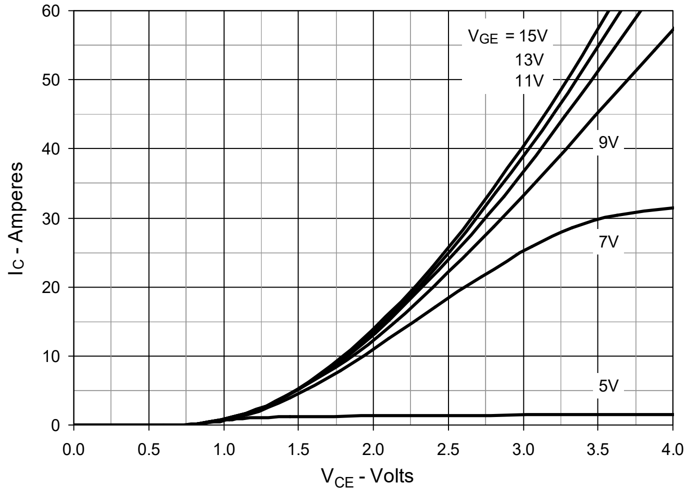

Fig. 2. Extended Output Characteristics @ T_J = 25ºC

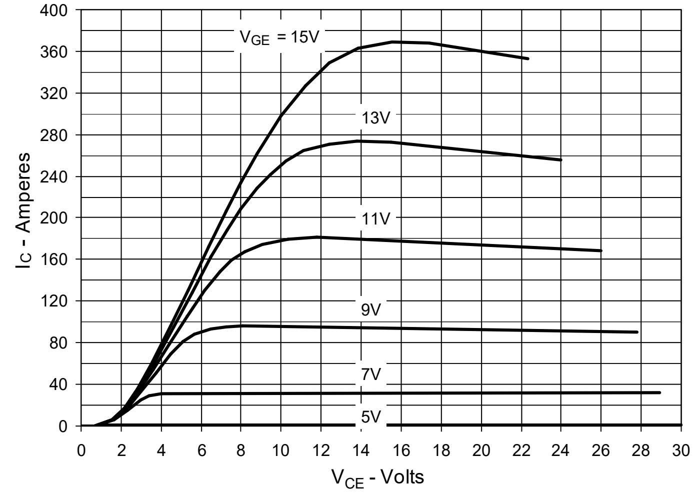

Fig. 3. Output Characteristics @ T_J = 125ºC

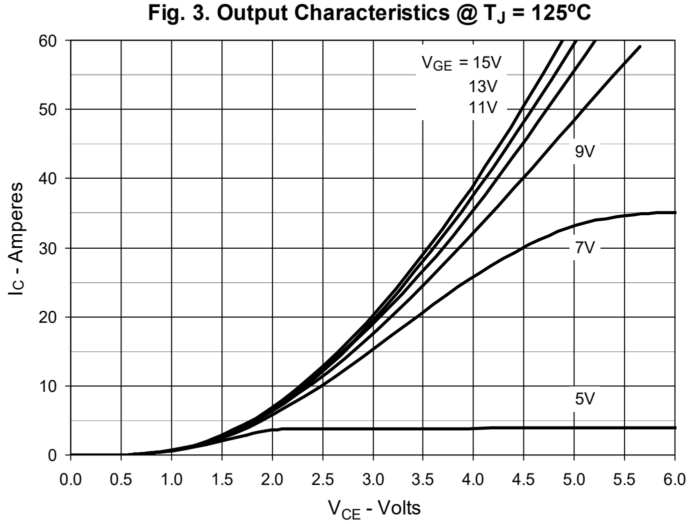

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

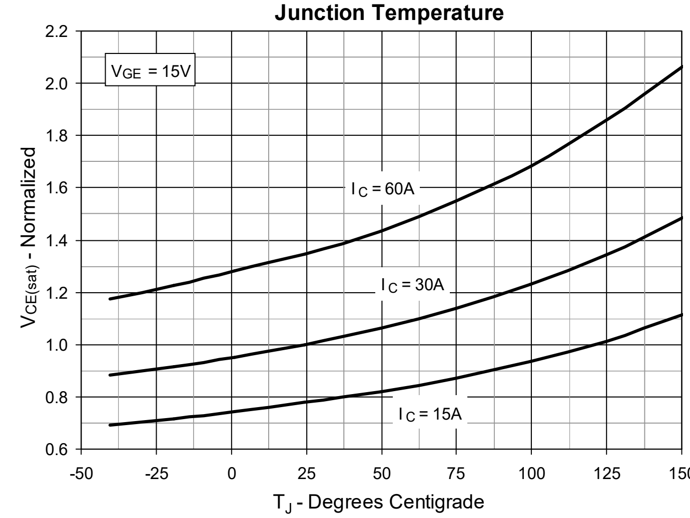

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

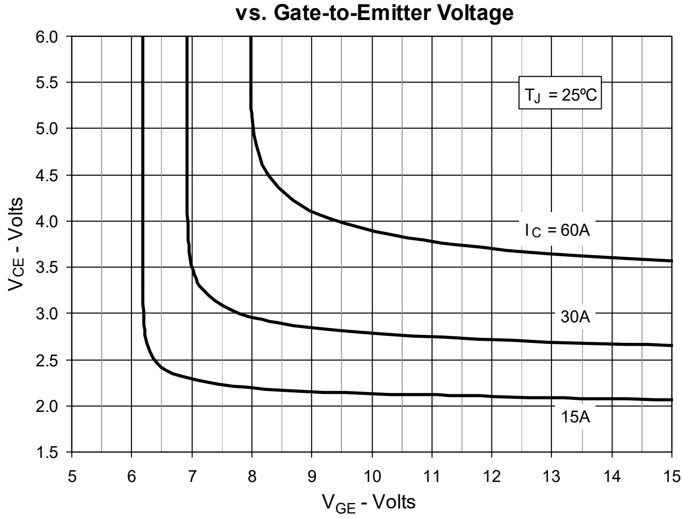

Fig. 6. Input Admittance

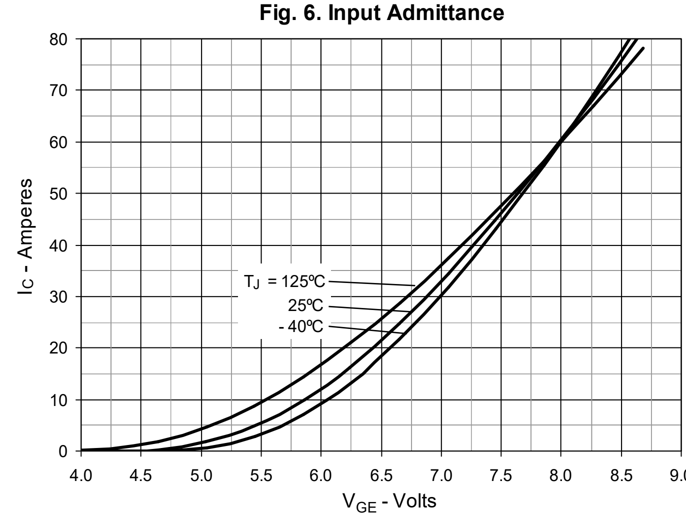

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Fig. 7. Transconductance

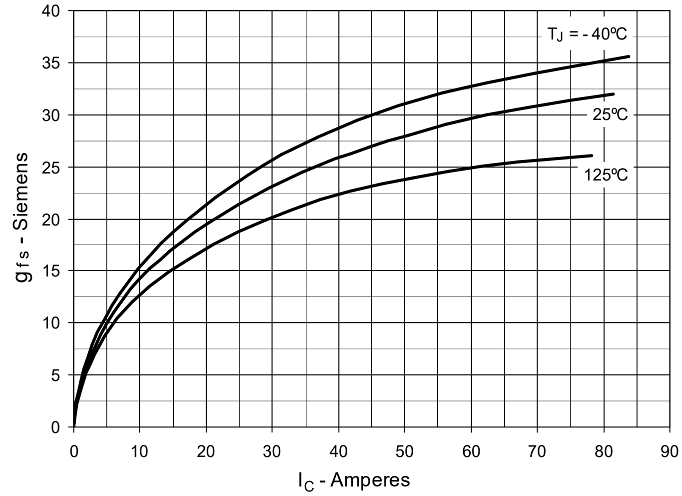

Fig. 8. Gate Charge

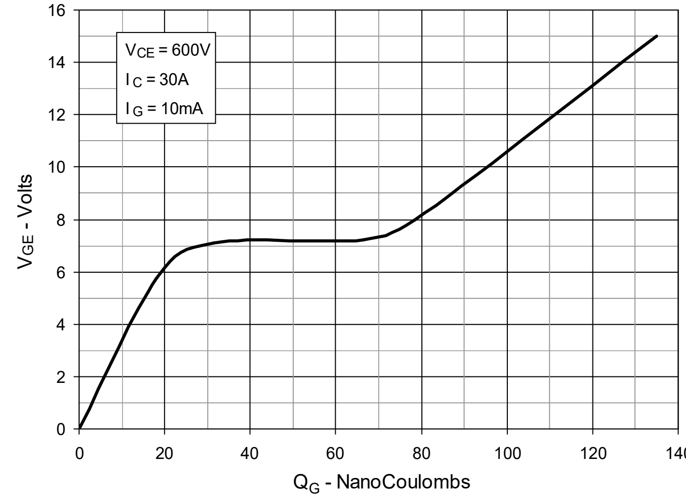

Fig. 9. Reverse-Bias Safe Operating Area

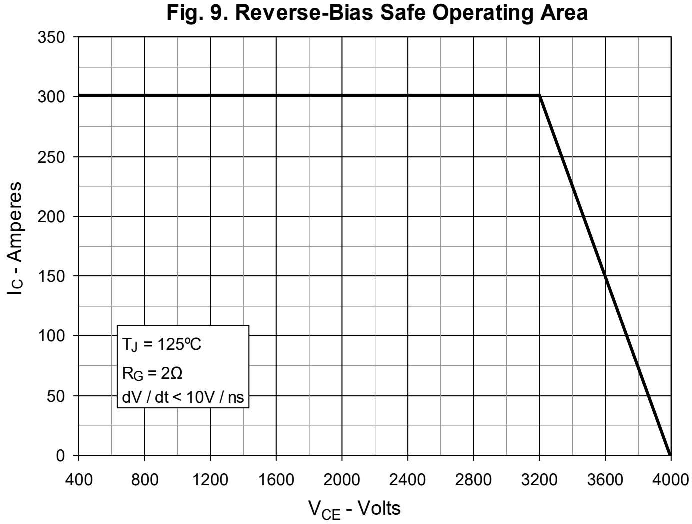

Fig. 10. Capacitance

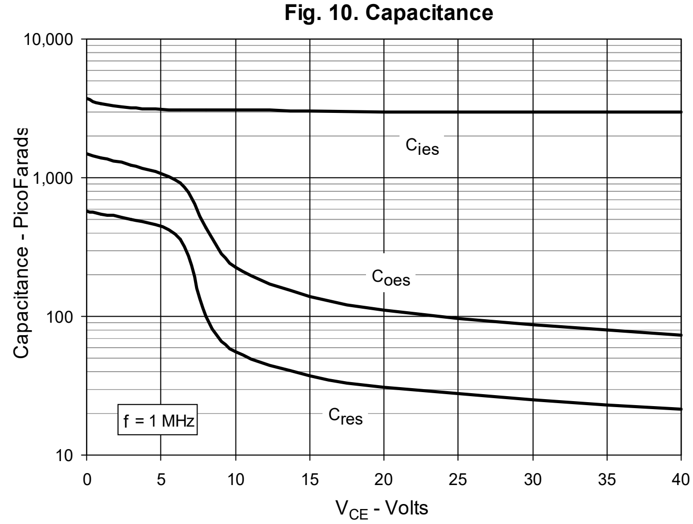

Fig. 11. Maximum Transient Thermal Impedance

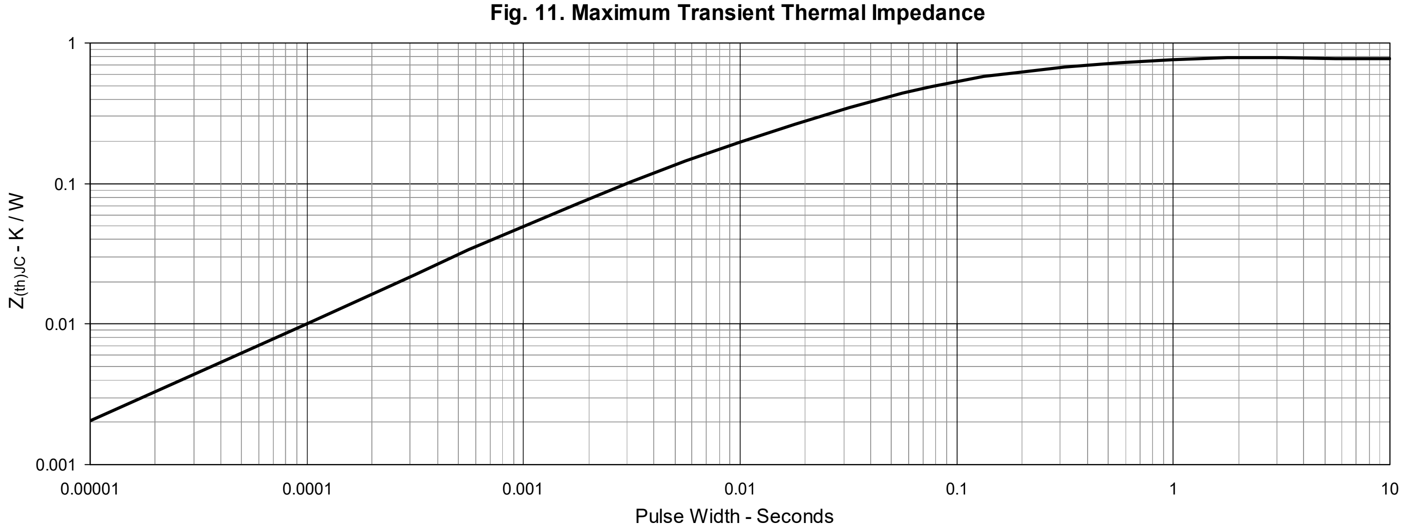

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Fig. 12. Resistive Turn-on
Rise Time vs. Junction Temperature

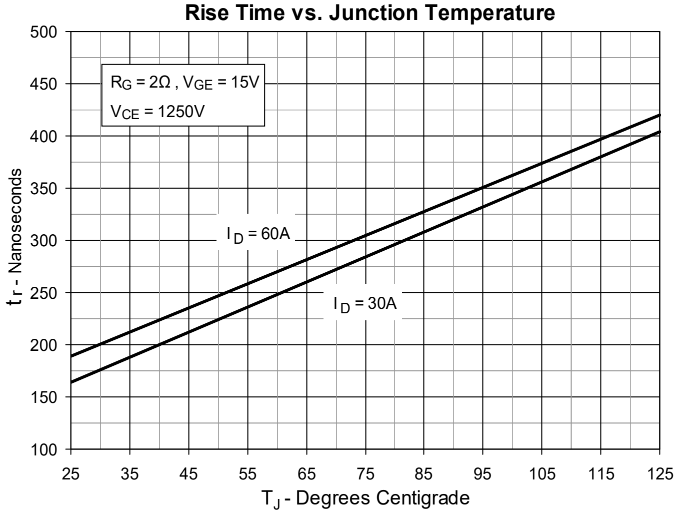


Fig. 13. Resistive Turn-on
Rise Time vs. Drain Current

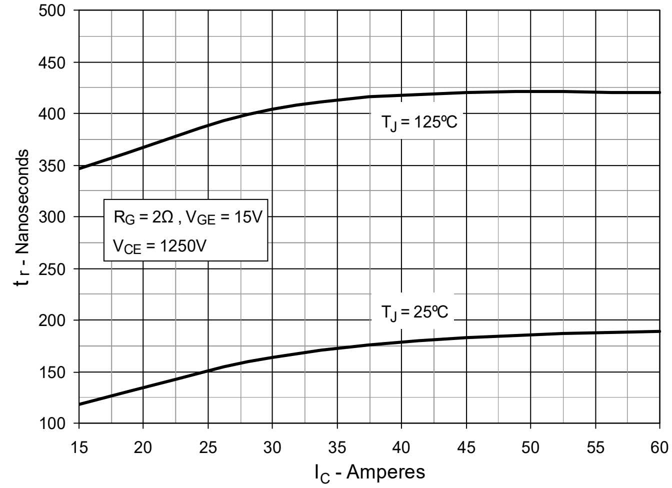


Fig. 14. Resistive Turn-on
Switching Times vs. Gate Resistance

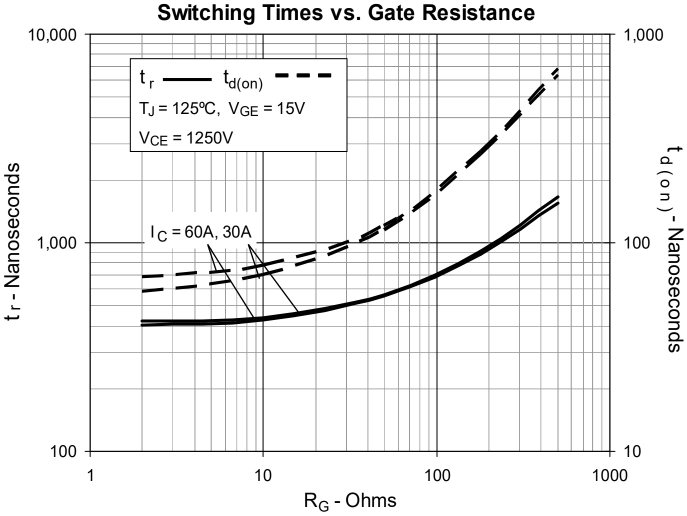


Fig. 15. Resistive Turn-off
Switching Times vs. Junction Temperature

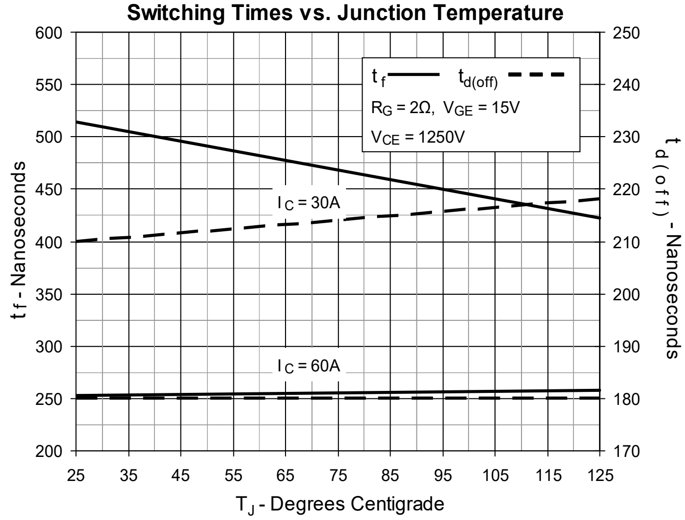


Fig. 16. Resistive Turn-off
Switching Times vs. Drain Current

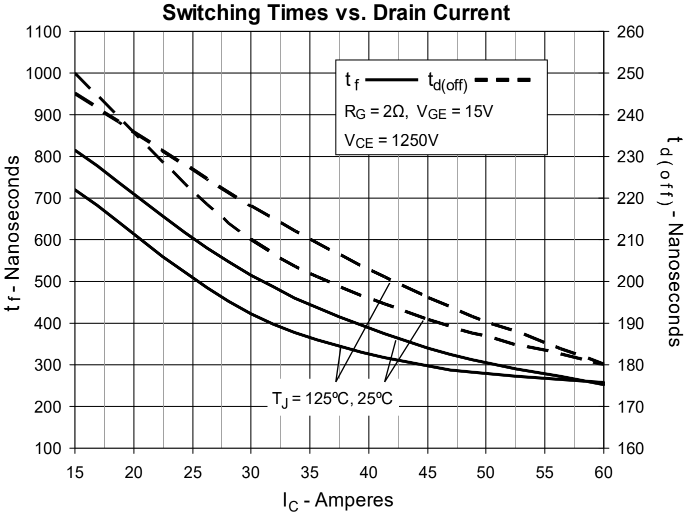
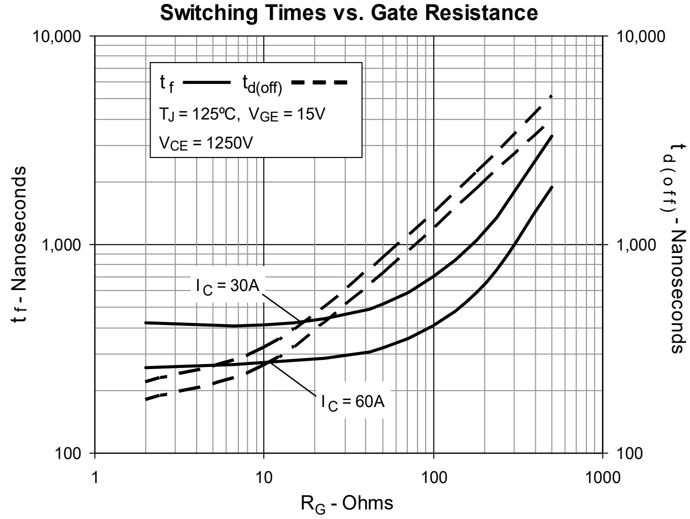


Fig. 17. Resistive Turn-off
Switching Times vs. Gate Resistance



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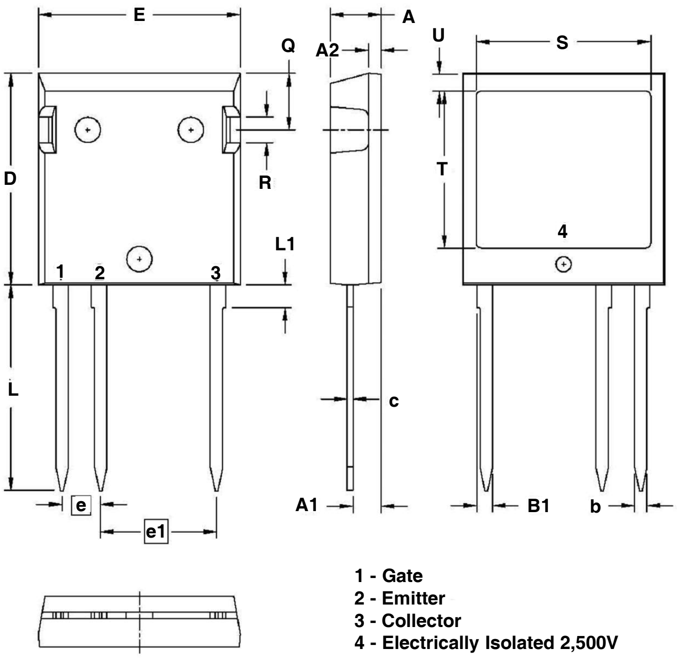
ISOPLUS I4-Pak™ (HV) Outline



1 - Gate
2 - Emitter
3 - Collector
4 - Electrically Isolated 2,500V

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

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