

# High Voltage XPT™ IGBT w/ Diode

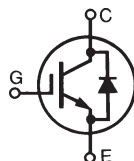
## IXYL50N170CV1

$$V_{CES} = 1700V$$

$$I_{C110} = 46A$$

$$V_{CE(sat)} \leq 3.7V$$

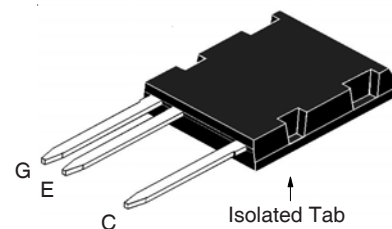
$$t_{fi(typ)} = 95ns$$



(Electrically Isolated Tab)

Symbol	Test Conditions	Maximum Ratings	
$V_{CES}$	$T_J = 25^\circ C$ to $175^\circ C$	1700	V
$V_{CGR}$	$T_J = 25^\circ C$ to $175^\circ C$ , $R_{GE} = 1M\Omega$	1700	V
$V_{GES}$	Continuous	$\pm 20$	V
$V_{GEM}$	Transient	$\pm 30$	V
$I_{C25}$	$T_C = 25^\circ C$	90	A
$I_{C110}$	$T_C = 110^\circ C$	46	A
$I_{F110}$	$T_C = 110^\circ C$	26	A
$I_{CM}$	$T_C = 25^\circ C$ , 1ms	325	A
<b>SSOA</b> <b>(RBSOA)</b>	$V_{GE} = 15V$ , $T_{VJ} = 150^\circ C$ , $R_G = 1\Omega$ Clamped Inductive Load	$I_{CM} = 200$ 1360	A V
$P_C$	$T_C = 25^\circ C$	580	W
$T_J$		-55 ... +175	$^\circ C$
$T_{JM}$		175	$^\circ C$
$T_{stg}$		-55 ... +175	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ C$
$T_{SOLD}$	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
$F_C$	Mounting Force	40..120 / 9..27	N/lb
$V_{ISOL}$	50/60 Hz, RM, t = 1min	2500	V~
<b>Weight</b>		8	g

### ISOPLUS i5-Pak™



G = Gate  
E = Emitter  
C = Collector

### Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4500V~ Electrical Isolation
- High Voltage Package
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

### Advantages

- Low Gate Drive Requirement
- High Power Density

### Applications

- UPS
- Motor Drives
- SMPS
- PFC Circuits
- High Frequency Power Inverters

Symbol	Test Conditions ( $T_J = 25^\circ C$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{CES}$	$I_C = 250\mu A$ , $V_{GE} = 0V$	1700		V
$V_{GE(th)}$	$I_C = 250\mu A$ , $V_{CE} = V_{GE}$	3.0		5.0 V
$I_{CES}$	$V_{CE} = V_{CES}$ , $V_{GE} = 0V$ $V_{CE} = 0.8 \cdot V_{CES}$ $T_J = 125^\circ C$			25 $\mu A$ 5 mA
$I_{GES}$	$V_{CE} = 0V$ , $V_{GE} = \pm 20V$			$\pm 100$ nA
$V_{CE(sat)}$	$I_C = 50A$ , $V_{GE} = 15V$ , Note 1 $T_J = 150^\circ C$		2.8 3.9	V V

Symbol Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)		Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$I_C = 50\text{A}, V_{CE} = 10\text{V}$ , Note 1	30	50	S
$R_{Gi}$	Gate Input Resistance		2.0	$\Omega$
$C_{ies}$	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		5500	pF
$C_{oes}$			380	pF
$C_{res}$			105	pF
$Q_{g(on)}$	$I_C = 50\text{A}, V_{GE} = 15\text{V}, V_{CE} = 0.5 \cdot V_{CES}$		260	nC
$Q_{ge}$			28	nC
$Q_{gc}$			110	nC
$t_{d(on)}$	<b>Inductive load, <math>T_J = 25^\circ\text{C}</math></b> $I_C = 50\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 0.5 \cdot V_{CES}, R_G = 1\Omega$ Note 2		20	ns
$t_{ri}$			44	ns
$E_{on}$			8.7	mJ
$t_{d(off)}$			180	ns
$t_{fi}$			95	ns
$E_{off}$			5.6	mJ
$t_{d(on)}$	<b>Inductive load, <math>T_J = 150^\circ\text{C}</math></b> $I_C = 50\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 0.5 \cdot V_{CES}, R_G = 1\Omega$ Note 2		22	ns
$t_{ri}$			40	ns
$E_{on}$			11.9	mJ
$t_{d(off)}$			236	ns
$t_{fi}$			160	ns
$E_{off}$			8.2	mJ
$R_{thJC}$				0.26 $^\circ\text{C/W}$
$R_{thCS}$		0.15		$^\circ\text{C/W}$

### Reverse Sonic Diode (FRD)

Symbol Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)		Characteristic Values		
		Min.	Typ.	Max.
$V_F$	$I_F = 50\text{A}, V_{GE} = 0\text{V}$ , Note 1 $T_J = 150^\circ\text{C}$		2.5 3.2	V V
$I_{RM}$	$I_F = 50\text{A}, V_{GE} = 0\text{V}, T_J = 150^\circ\text{C}$ $-di_F/dt = 500\text{A}/\mu\text{s}, V_R = 1200\text{V}$		40	A
$t_{rr}$			255	ns
$R_{thJC}$				0.83 $^\circ\text{C/W}$

#### Notes:

1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .
2. Switching times & energy losses may increase for higher  $V_{CE}$ (Clamp),  $T_J$  or  $R_G$ .

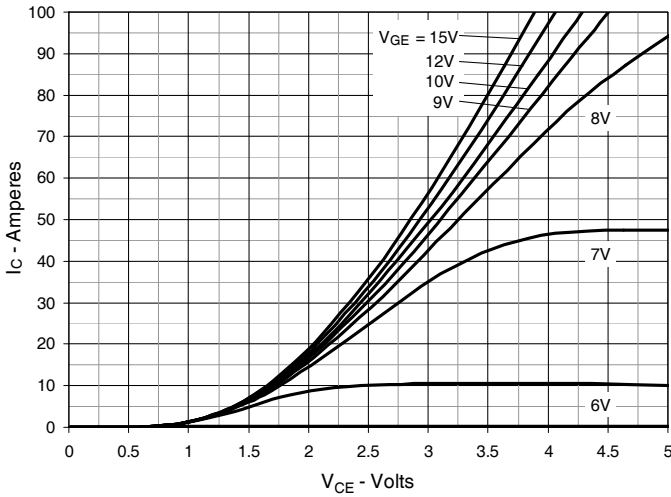
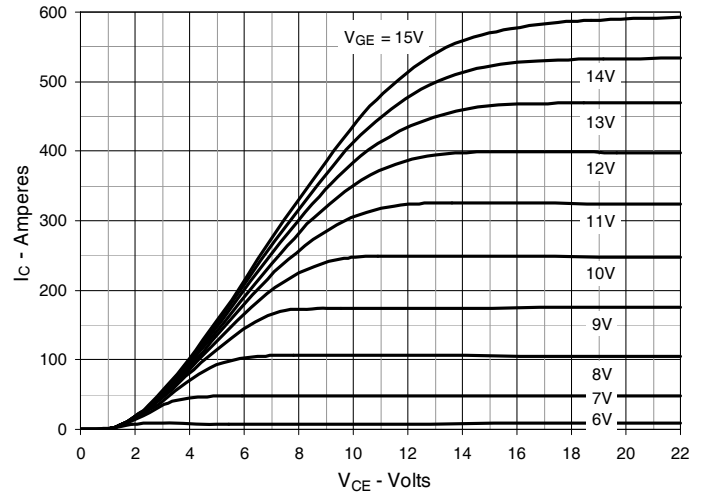
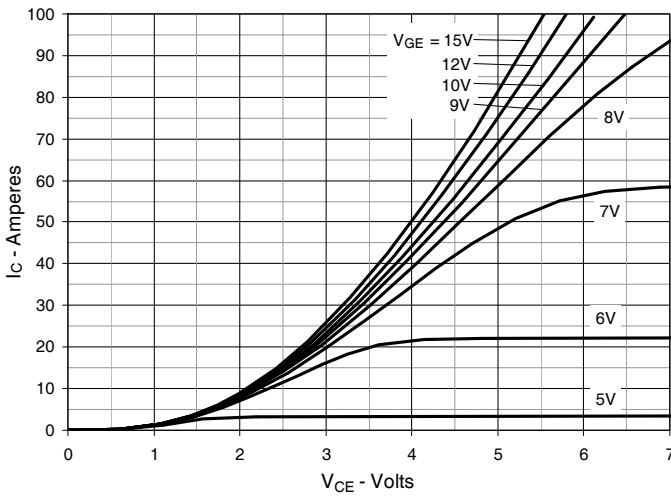
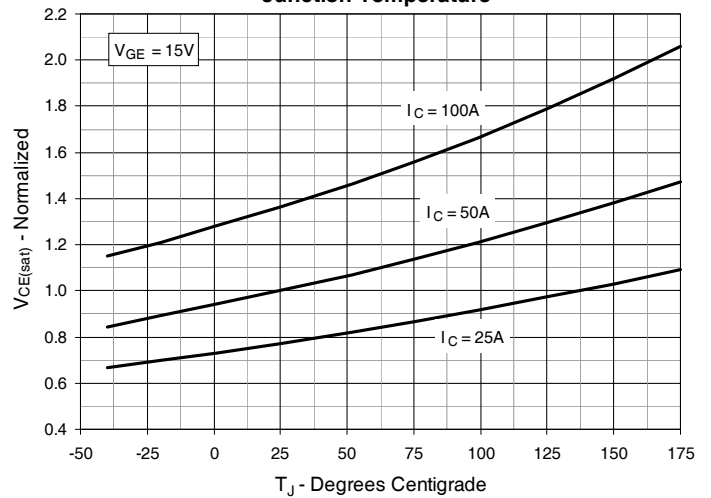
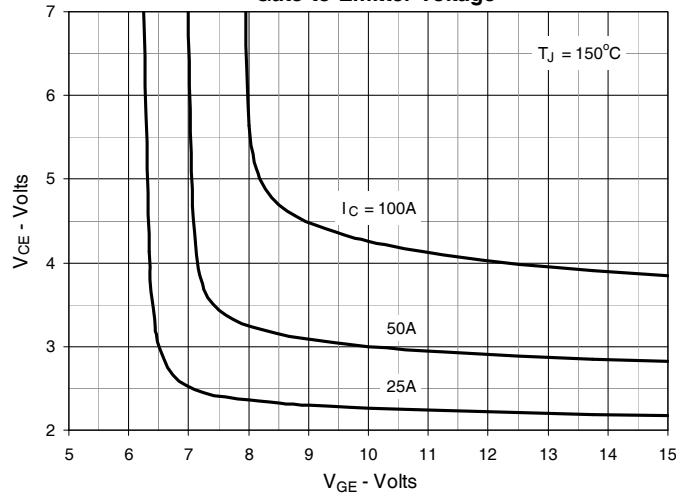
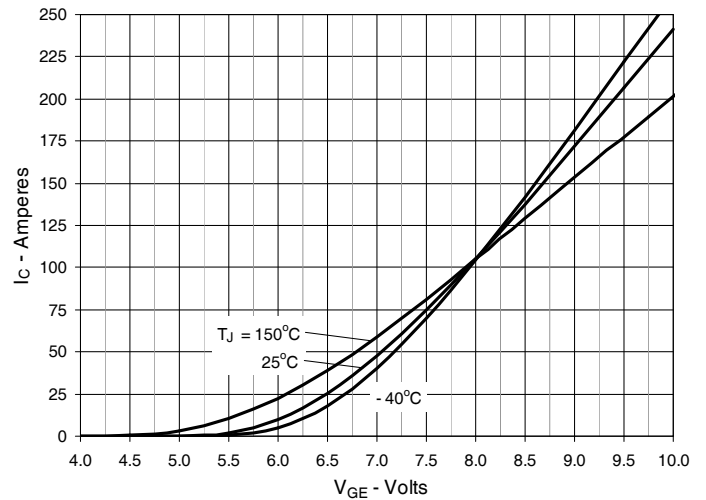
### ADVANCE TECHNICAL INFORMATION

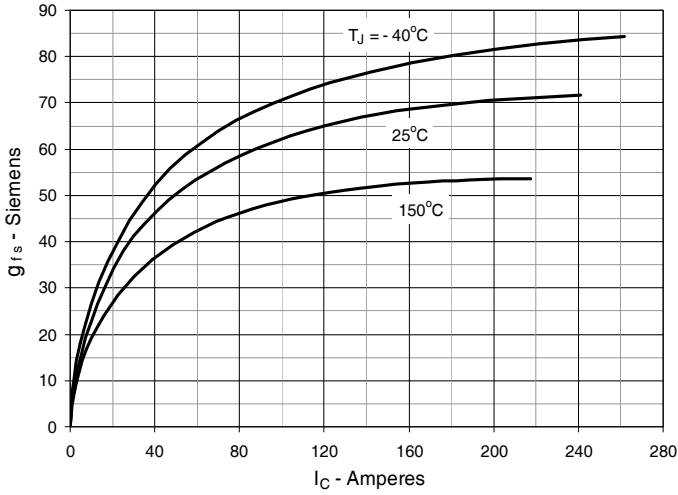
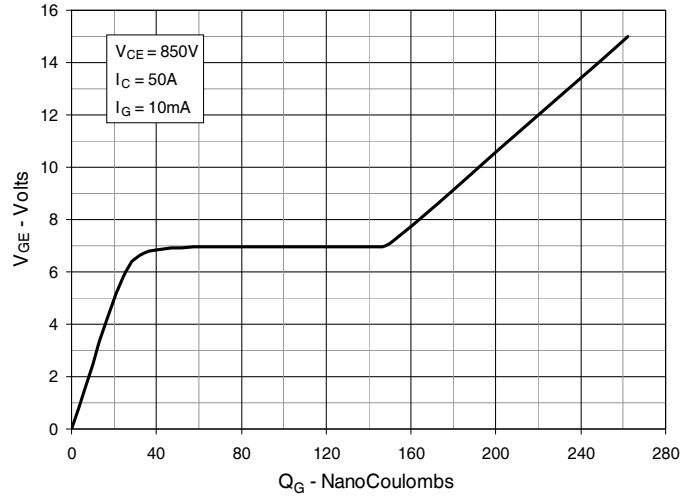
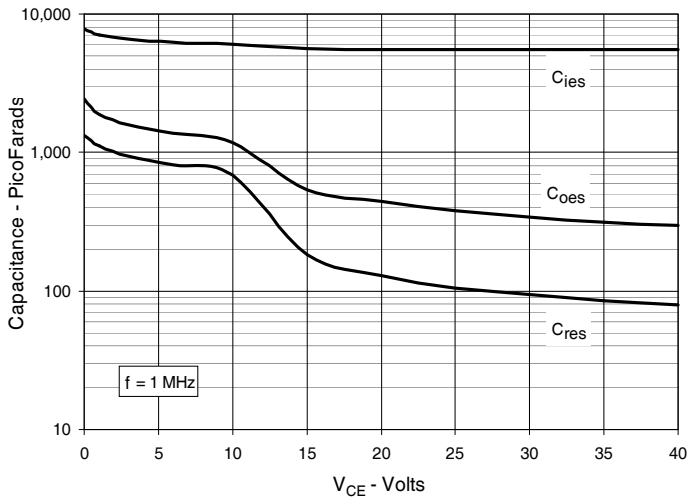
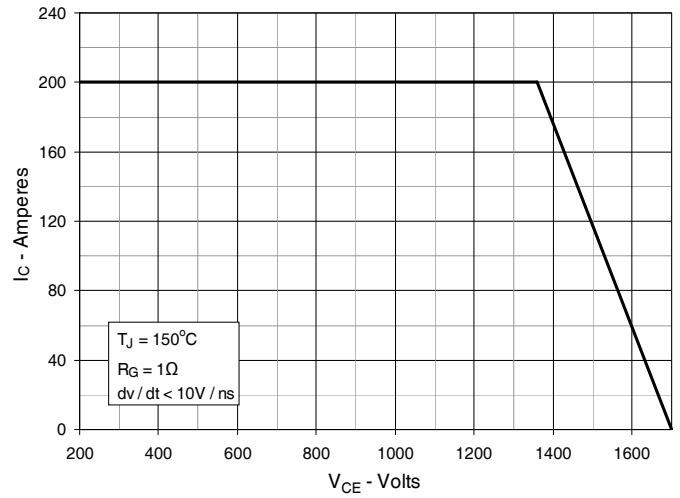
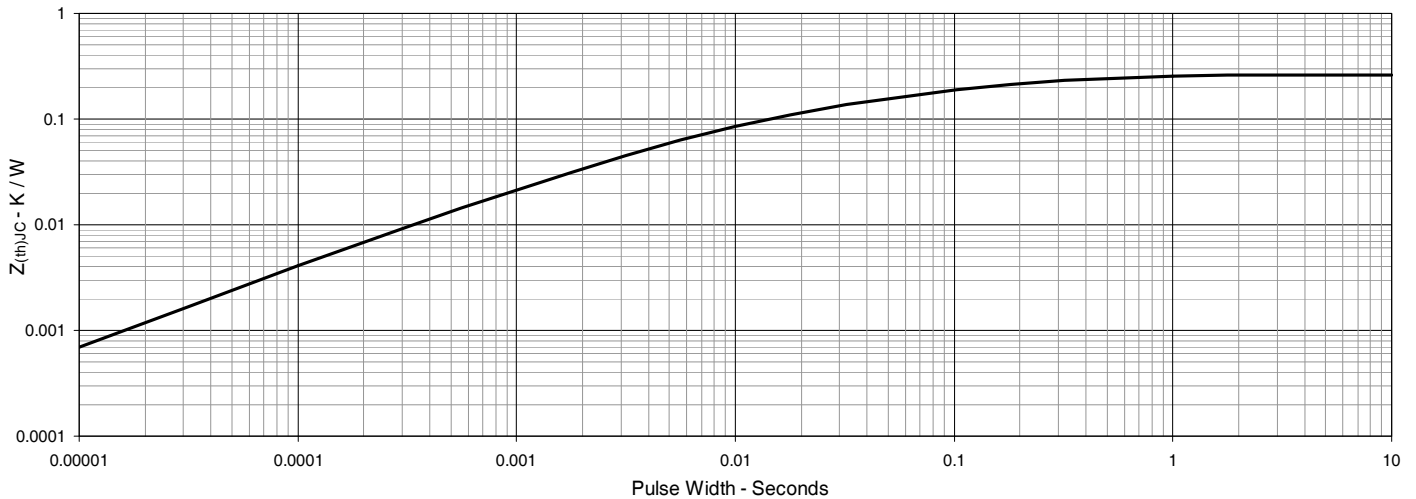
The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

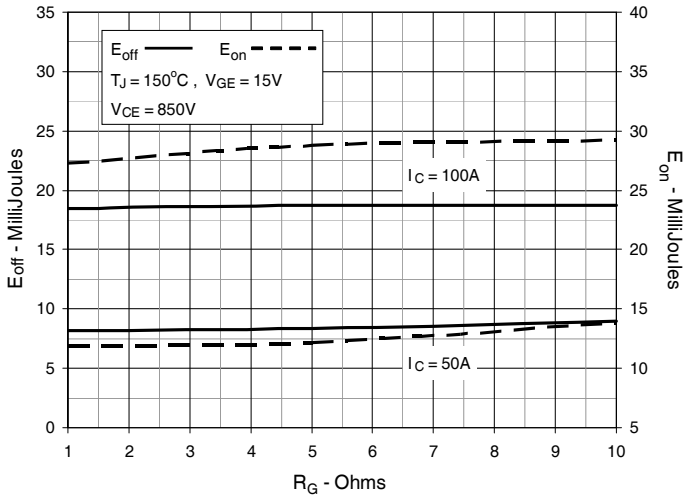
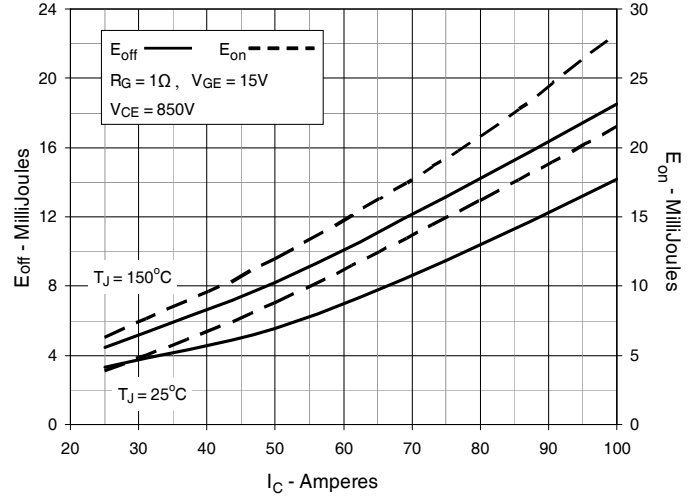
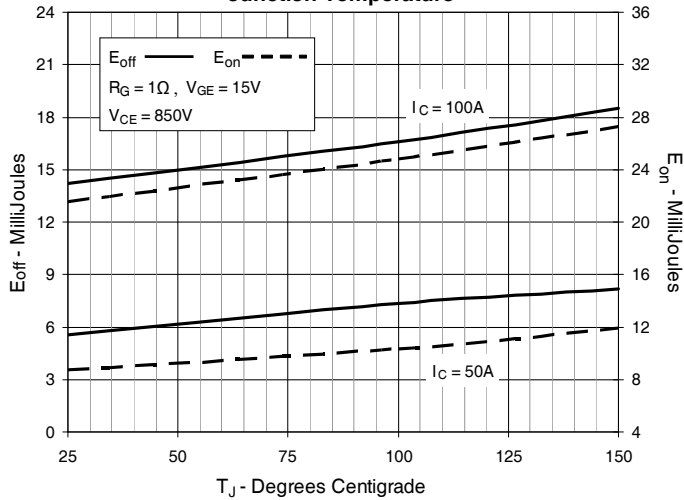
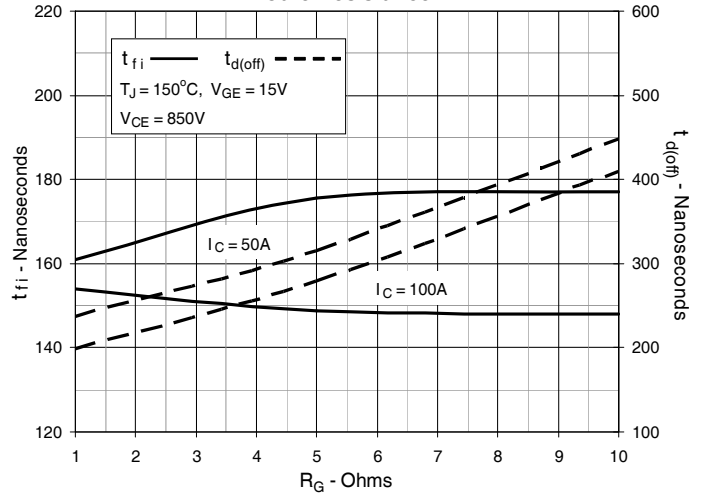
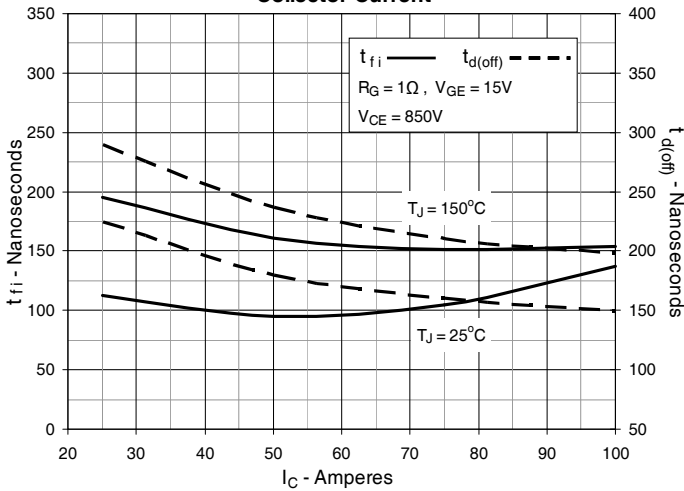
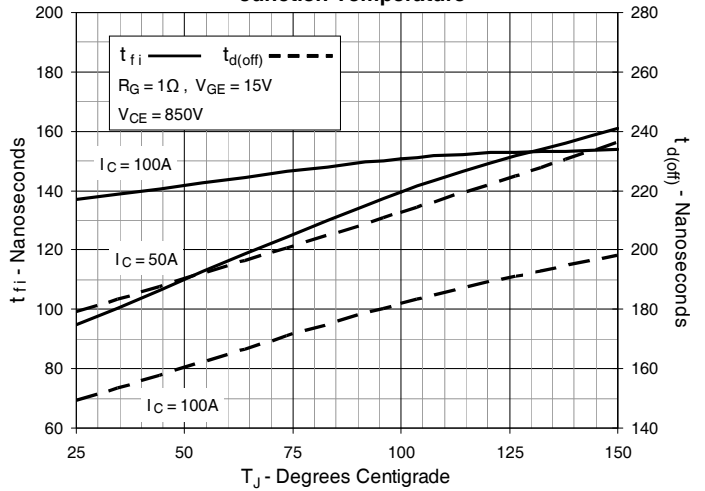
IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

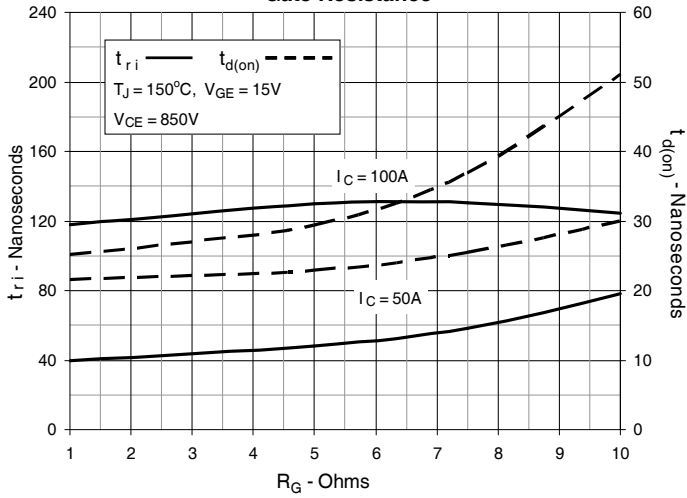
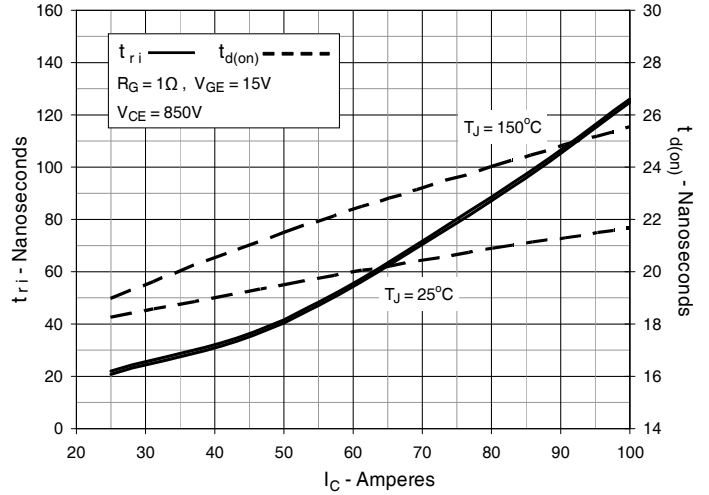
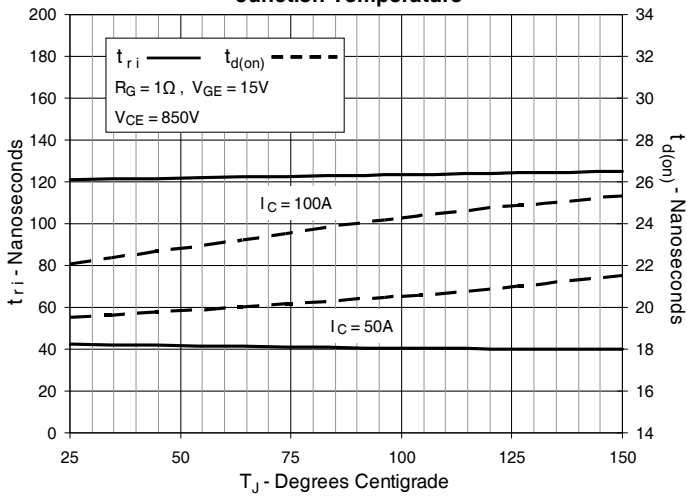
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

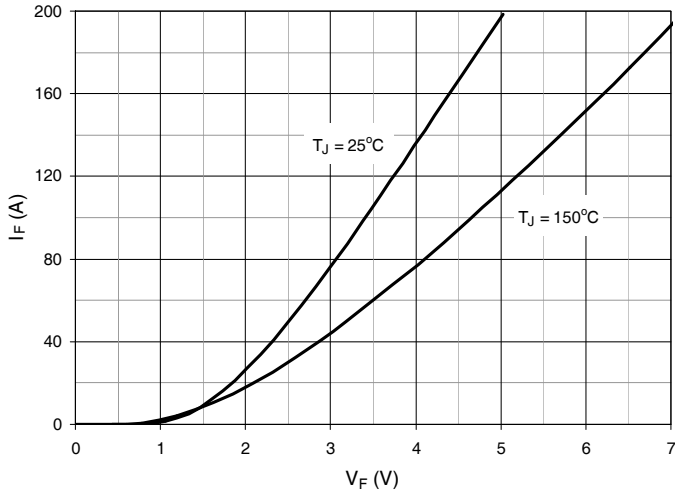
**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 3. Output Characteristics @  $T_J = 150^\circ\text{C}$** 

**Fig. 4. Dependence of  $V_{CE(sat)}$  on Junction Temperature**

**Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage**

**Fig. 6. Input Admittance**


**Fig. 7. Transconductance**

**Fig. 8. Gate Charge**

**Fig. 9. Capacitance**

**Fig. 10. Reverse-Bias Safe Operating Area**

**Fig. 11. Maximum Transient Thermal Impedance (IGBT)**


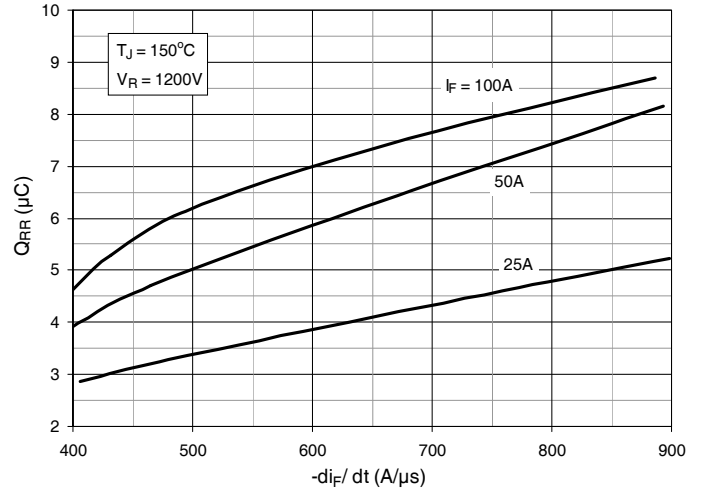
**Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance**

**Fig. 13. Inductive Switching Energy Loss vs. Collector Current**

**Fig. 14. Inductive Switching Energy Loss vs. Junction Temperature**

**Fig. 15. Inductive Turn-off Switching Times vs. Gate Resistance**

**Fig. 16. Inductive Turn-off Switching Times vs. Collector Current**

**Fig. 17. Inductive Turn-off Switching Times vs. Junction Temperature**


**Fig. 19. Inductive Turn-on Switching Times vs. Gate Resistance**

**Fig. 20. Inductive Turn-on Switching Times vs. Collector Current**

**Fig. 21. Inductive Turn-on Switching Times vs. Junction Temperature**


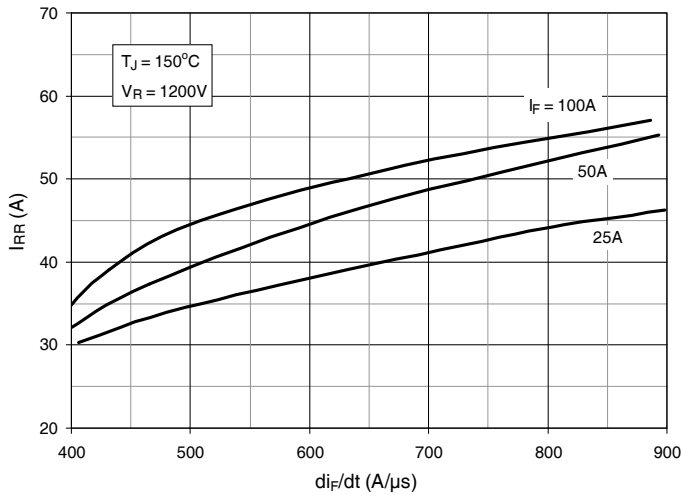
**Fig. 22. Diode Forward Characteristics**



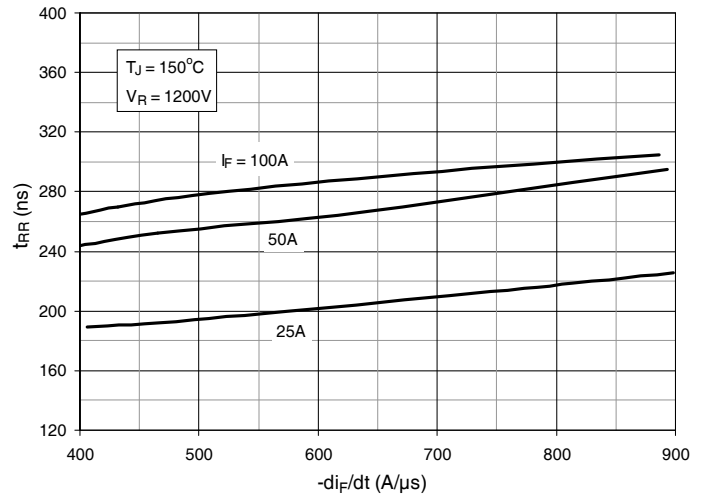
**Fig. 23. Reverse Recovery Charge vs.  $-di_F/dt$**



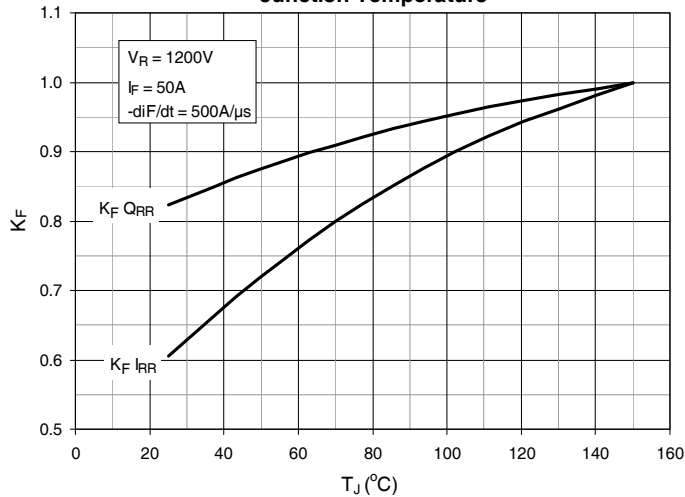
**Fig. 23. Reverse Recovery Current vs.  $-di_F/dt$**



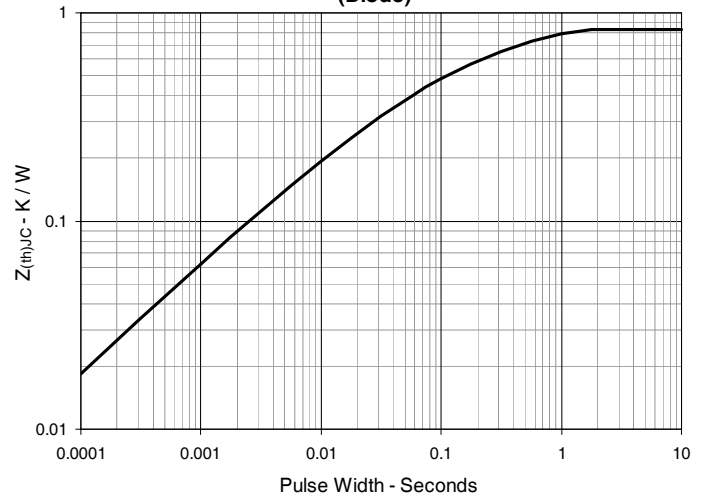
**Fig. 24. Reverse Recovery Time vs.  $-di_F/dt$**

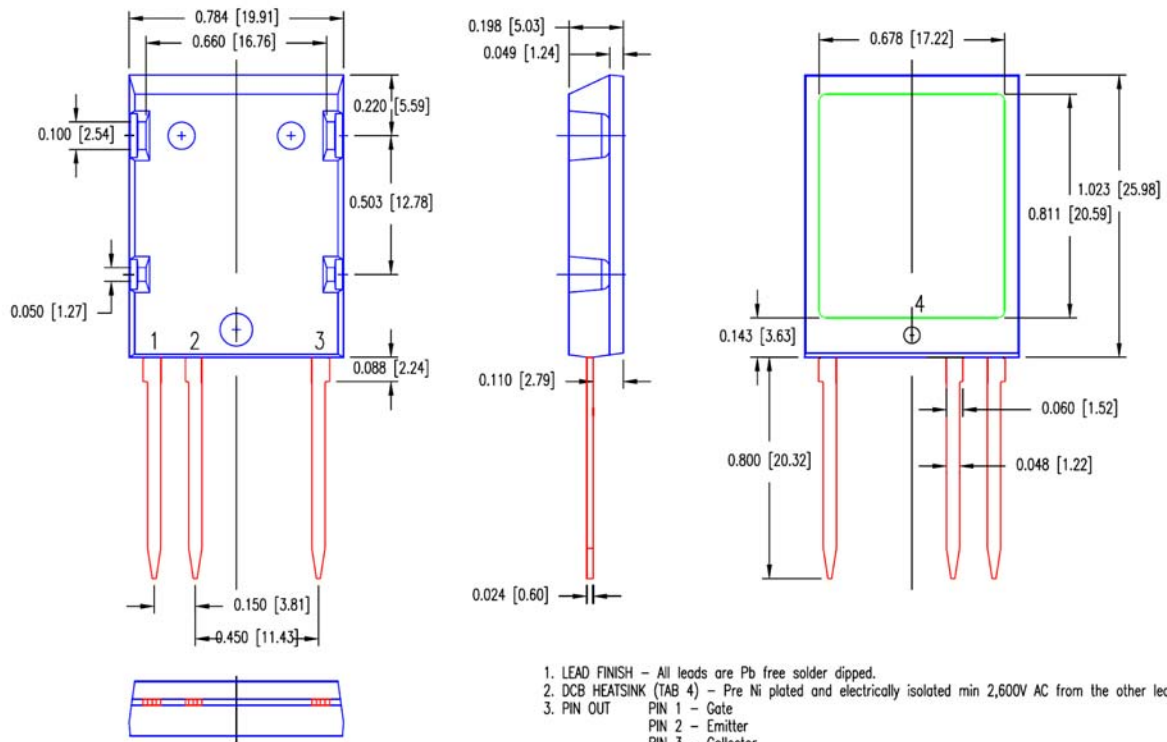


**Fig. 25. Dynamic Parameters  $Q_{RR}$ ,  $I_{RR}$  vs. Junction Temperature**



**Fig. 26. Maximum Transient Thermal Impedance (Diode)**



**ISOPLUS i5-Pak™ (IXYL) Outline**


1. LEAD FINISH – All leads are Pb free solder dipped.
2. DCB HEATSINK (TAB 4) – Pre Ni plated and electrically isolated min 2,600V AC from the other leads.
3. PIN OUT
  - PIN 1 – Gate
  - PIN 2 – Emitter
  - PIN 3 – Collector
  - TAP 4 – Isolated DCB Cu





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