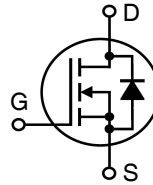


**Q3-Class
HiperFET™
Power MOSFET**

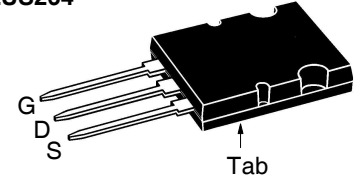
IXFB62N80Q3

V_{DSS} = 800V
I_{D25} = 62A
R_{DS(on)} ≤ 140mΩ
t_{rr} ≤ 300ns

N-Channel Enhancement Mode
 Fast Intrinsic Rectifier
 Avalanche Rated



PLUS264™



G = Gate D = Drain
 S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 150°C	800	V
V _{DGR}	T _J = 25°C to 150°C, R _{GS} = 1MΩ	800	V
V _{GSS}	Continuous	±30	V
V _{GSM}	Transient	±40	V
I _{D25}	T _C = 25°C	62	A
I _{DM}	T _C = 25°C, Pulse Width Limited by T _{JM}	180	A
I _A	T _C = 25°C	62	A
E _{AS}	T _C = 25°C	5	J
dv/dt	I _S ≤ I _{DM} , V _{DD} ≤ V _{DSS} , T _J ≤ 150°C	50	V/ns
P _D	T _C = 25°C	1560	W
T _J		-55 ... +150	°C
T _{JM}		150	°C
T _{stg}		-55 ... +150	°C
T _L	Maximum Lead Temperature for Soldering	300	°C
T _{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
F _C	Mounting Force	30..120/6.7..27	N/lb.
Weight		10	g

Features

- Low Intrinsic Gate Resistance
- Low Package Inductance
- Avalanche Rated
- Fast Intrinsic Rectifier
- Low R_{DS(on)} and Q_G

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- DC Choppers
- Temperature and Lighting Controls

Symbol	Test Conditions (T _J = 25°C Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV _{DSS}	V _{GS} = 0V, I _D = 3mA	800		V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 8mA	3.5		6.5 V
I _{GSS}	V _{GS} = ±30V, V _{DS} = 0V			±200 nA
I _{DSS}	V _{DS} = 0.8 • V _{DSS} , V _{GS} = 0V T _J = 125°C			50 μA 4 mA
R _{DS(on)}	V _{GS} = 10V, I _D = 0.5 • I _{D25} , Note 1			140 mΩ

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}, I_D = I_D = 0.5 \cdot I_{D25}$, Note 1	28	48	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		13.6	nF
C_{oss}			1260	pF
C_{rss}			100	pF
R_{Gi}	Gate Input Resistance		0.13	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 1\Omega$ (External)		54	ns
t_r			20	ns
$t_{d(off)}$			62	ns
t_f			11	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = I_D = 0.5 \cdot I_{D25}$		270	nC
Q_{gs}			90	nC
Q_{gd}			120	nC
R_{thJC}				0.08 $^\circ\text{C/W}$
R_{thCS}		0.13		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			62 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			250 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 31\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			300 ns
Q_{RM}			1.6	μC
I_{RM}			13.4	A

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
by one or more of the following U.S. patents:	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

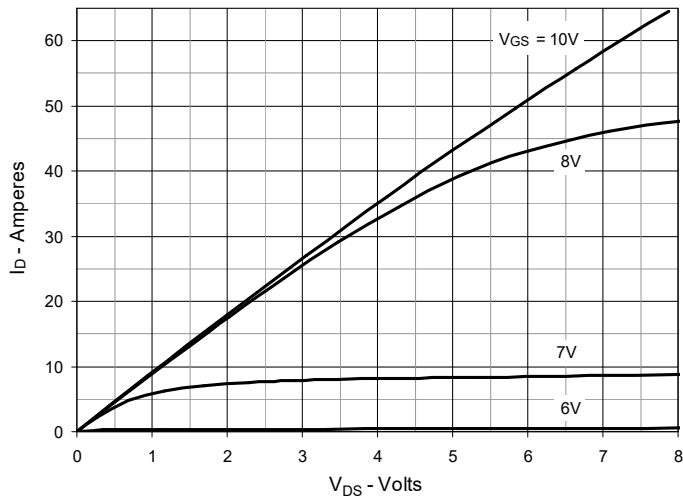
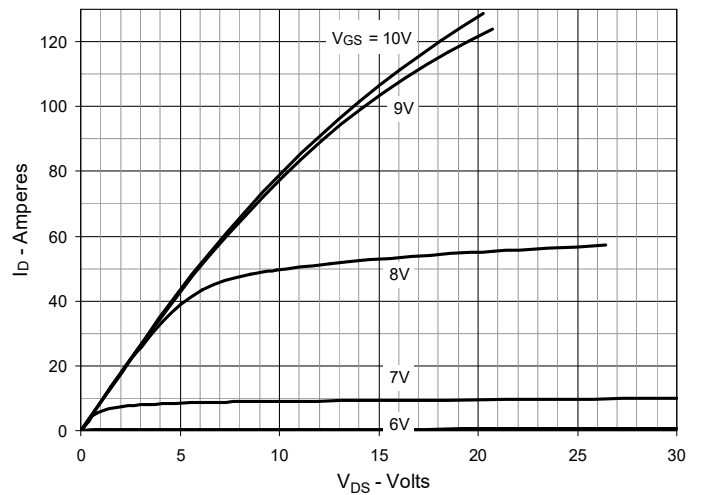
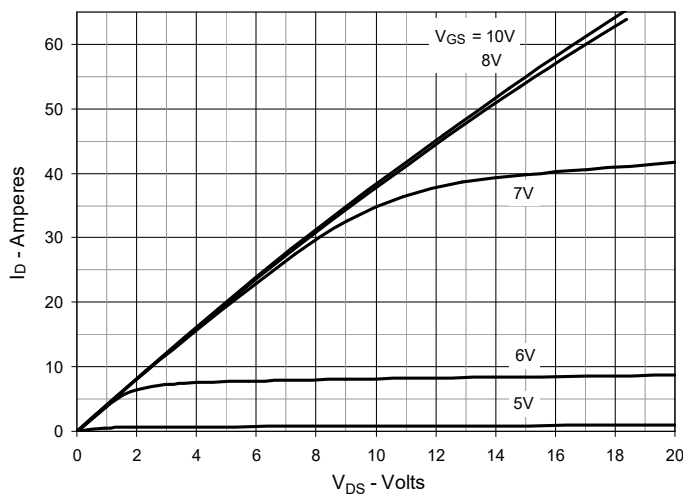
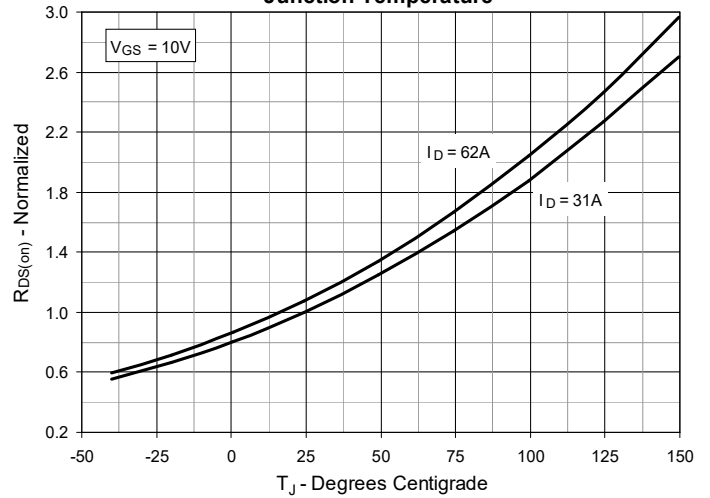
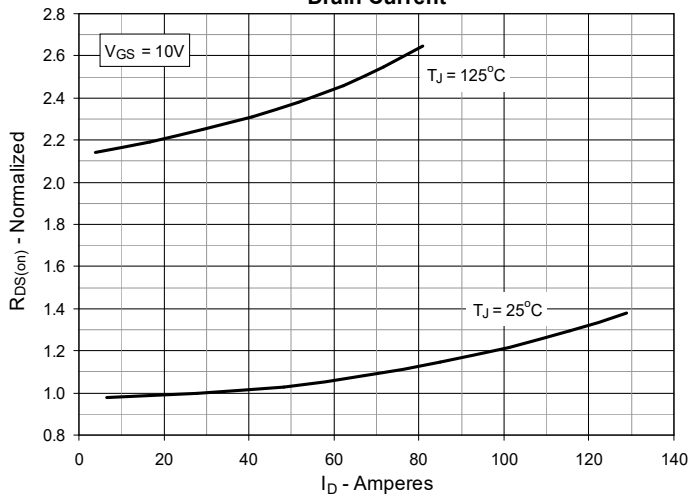
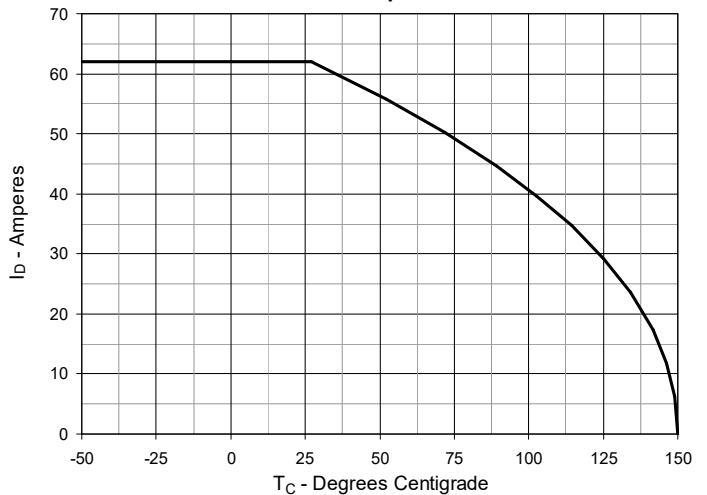
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 31\text{A}$ Value vs. Junction Temperature

Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 31\text{A}$ Value vs. Drain Current

Fig. 6. Maximum Drain Current vs. Case Temperature


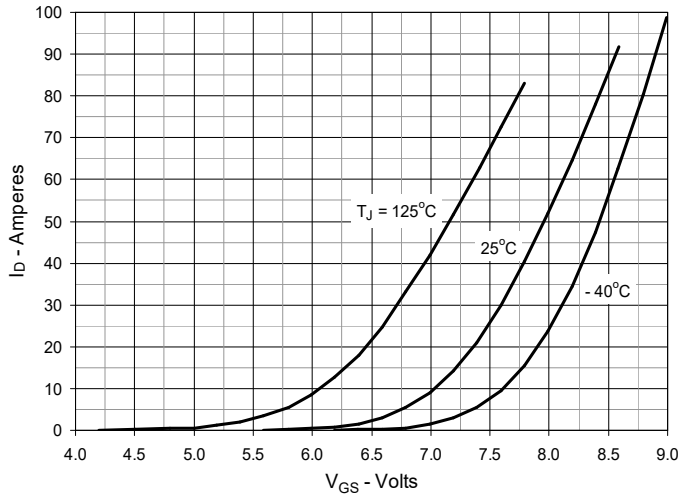
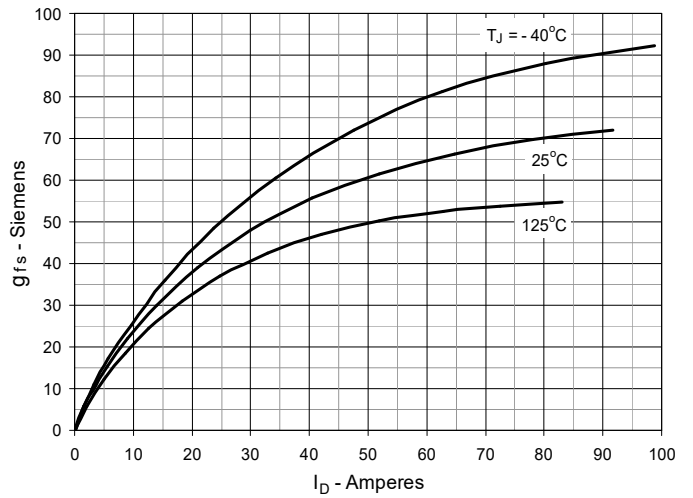
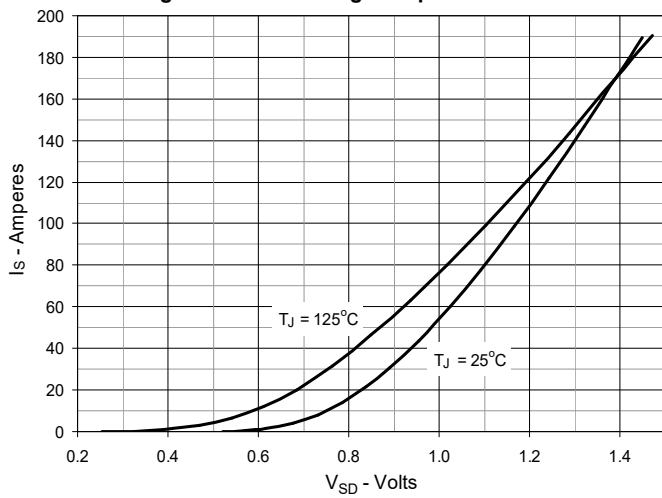
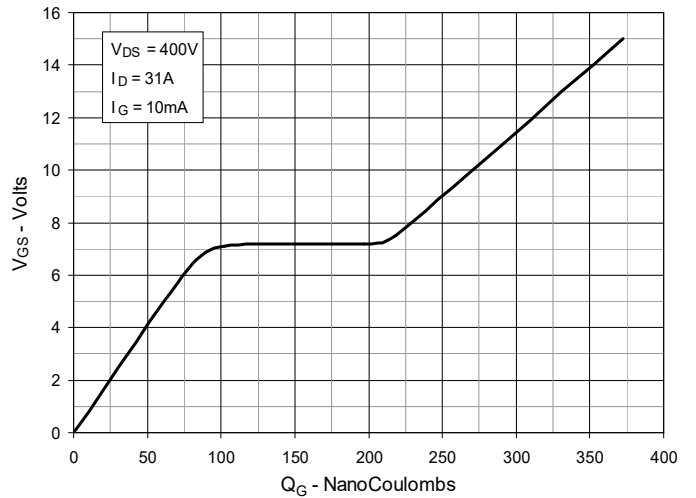
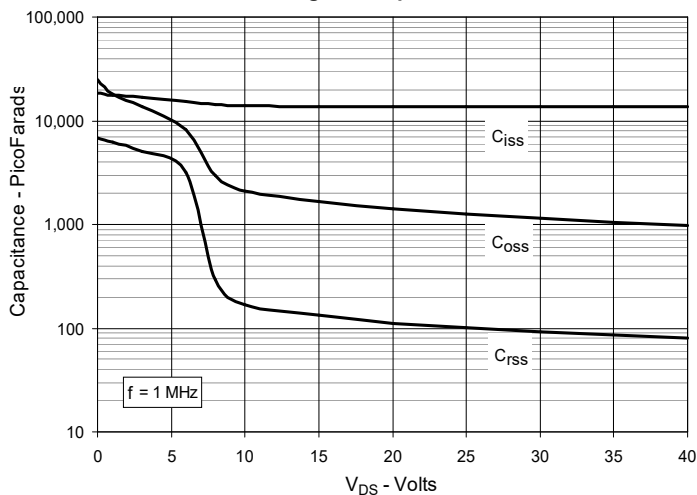
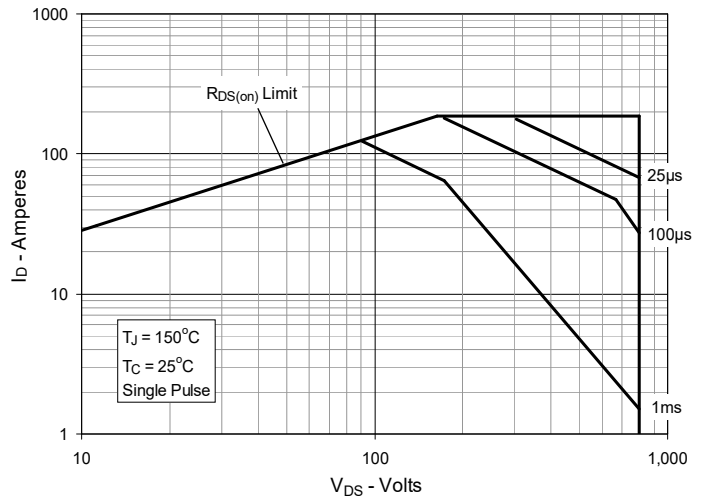
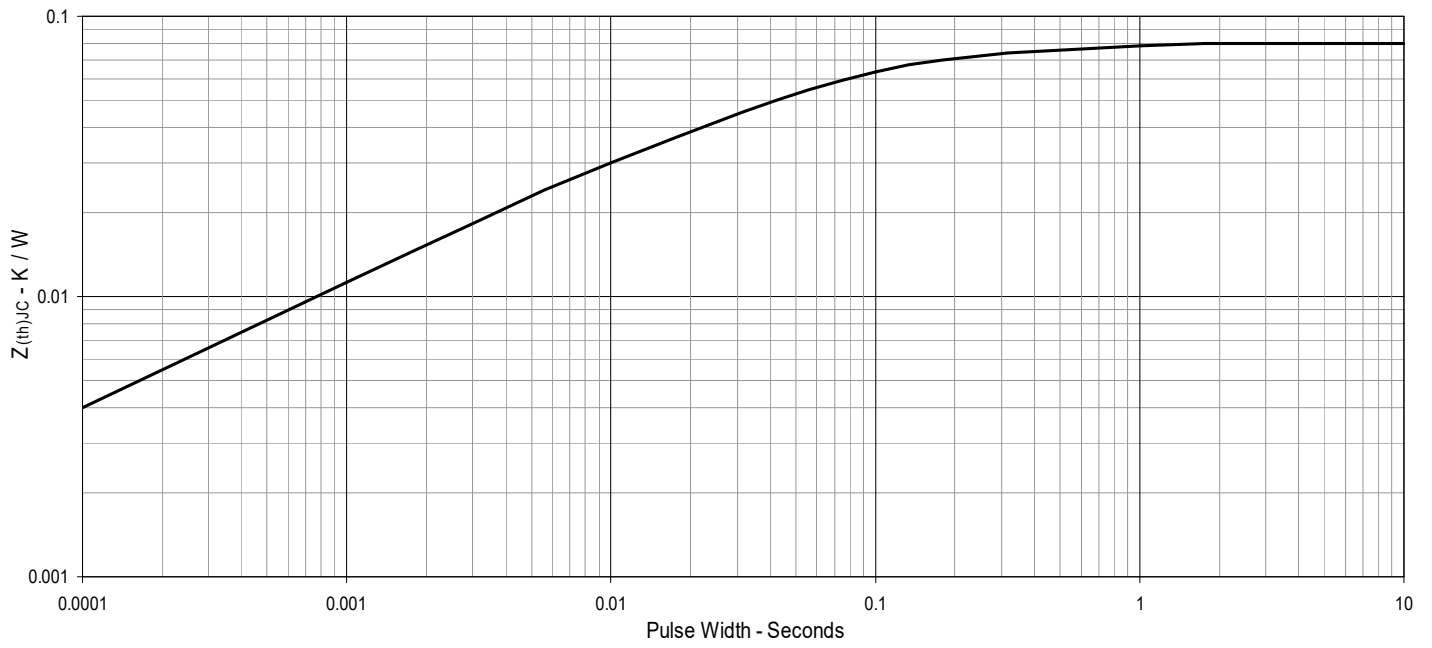
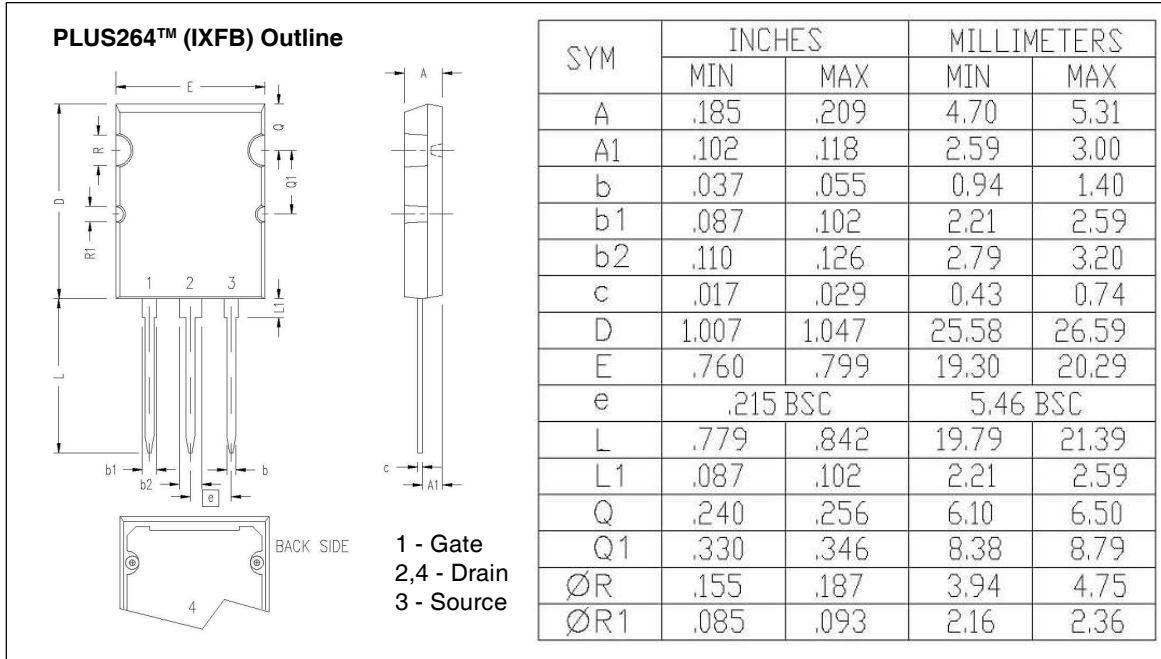
Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Forward Voltage Drop of Intrinsic Diode

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Forward-Bias Safe Operating Area


Fig. 13. Maximum Transient Thermal Impedance







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