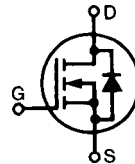


HiPerFET™ Power MOSFETs

~~IXFH/IXFM35N30~~
IXFH40N30
IXFM40N30

N-Channel Enhancement Mode
High dv/dt, Low t_{rr}, HDMOS™ Family

Obsolete:
IXFM35N30

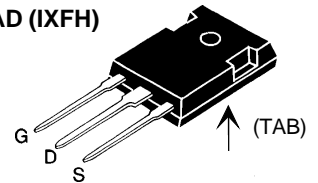


V _{DSS}	I _{D25}	R _{DS(on)}
300 V	35 A	100 mΩ
300 V	40 A	85 mΩ
300 V	40 A	88 mΩ

t_{rr} ≤ 200 ns

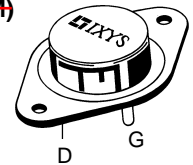
Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 150°C	300	V
V _{DGR}	T _J = 25°C to 150°C; R _{GS} = 1 MΩ	300	V
V _{GS}	Continuous	±20	V
V _{GSM}	Transient	±30	V
I _{D25}	T _C = 25°C	35N30 40N30	35 40 A A
I _{DM}	T _C = 25°C, pulse width limited by T _{JM}	35N30 40N30	140 160 A A
I _{AR}	T _C = 25°C	35N30 40N30	35 40 A A
E _{AR}	T _C = 25°C	30	mJ
dv/dt	I _S ≤ I _{DM} , di/dt ≤ 100 A/μs, V _{DD} ≤ V _{DSS} , T _J ≤ 150°C, R _G = 2 Ω	5	V/ns
P _D	T _C = 25°C	300	W
T _J		-55 ... +150	°C
T _{JM}		150	°C
T _{stg}		-55 ... +150	°C
T _L	1.6 mm (0.062 in.) from case for 10 s	300	°C
M _d	Mounting torque	1.13/10	Nm/lb.in.
Weight		TO-204 = 18 g, TO-247 = 6 g	

TO-247 AD (IXFH)



TO-204 AE (IXFM)

Package unavailable



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard packages
- Low R_{DS(on)} HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
 - easy to drive and to protect
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls
- Low voltage relays

Advantages

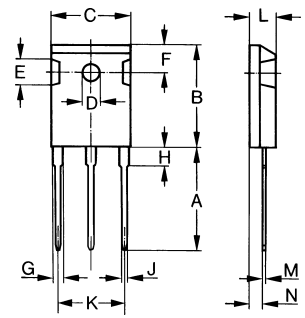
- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values (T _J = 25°C, unless otherwise specified)		
		min.	typ.	max.
V _{DSS}	V _{GS} = 0 V, I _D = 250 μA	300		V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 4 mA	2		V
I _{GSS}	V _{GS} = ±20 V _{DC} , V _{DS} = 0			±100 nA
I _{DSS}	V _{DS} = 0.8 • V _{DSS} , V _{GS} = 0 V			200 μA 1 mA
R _{DS(on)}	V _{GS} = 10 V, I _D = 0.5 I _{D25}			0.100 Ω 0.085 Ω 0.088 Ω
	Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			

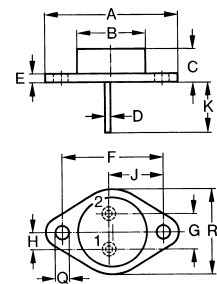
Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)			
		min.	typ.	max.	
g_{fs}	$V_{DS} = 10\text{ V}; I_D = 0.5 I_{D25}$, pulse test	22	25	S	
C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		4800	pF	
C_{oss}			745	pF	
C_{rss}			280	pF	
$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 I_{D25}$ $R_G = 2\ \Omega$ (External)		20	30	ns
t_r			60	90	ns
$t_{d(off)}$			75	100	ns
t_f			45	90	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 I_{D25}$		177	200	nC
Q_{gs}			28	50	nC
Q_{gd}			78	105	nC
R_{thJC}				0.42	K/W
R_{thCK}			0.25		K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)			
		min.	typ.	max.	
I_S	$V_{GS} = 0\text{ V}$	35N30 40N30		35 40	A A
I_{SM}	Repetitive; pulse width limited by T_{JM}	35N30 40N30		140 160	A A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			1.5	V
t_{rr}	$I_F = I_S, -di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 100\text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$		200 350	ns ns

TO-247 AD (IXFH) Outline


Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	19.81	20.32	0.780	0.800
B	20.80	21.46	0.819	0.845
C	15.75	16.26	0.610	0.640
D	3.55	3.65	0.140	0.144
E	4.32	5.49	0.170	0.216
F	5.4	6.2	0.212	0.244
G	1.65	2.13	0.065	0.084
H	-	4.5	-	0.177
J	1.0	1.4	0.040	0.055
K	10.8	11.0	0.426	0.433
L	4.7	5.3	0.185	0.209
M	0.4	0.8	0.016	0.031
N	1.5	2.49	0.087	0.102

TO-204 AE (IXFM) Outline


Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	38.61	39.12	1.520	1.540
B	-	22.22	-	0.875
C	6.40	11.40	0.252	0.449
D	1.45	1.60	0.057	0.063
E	1.52	3.43	0.060	0.135
F	30.15	BSC	1.187	BSC
G	10.67	11.17	0.420	0.440
H	5.21	5.71	0.205	0.225
J	16.64	17.14	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.16	26.66	0.991	1.050

Fig.1. Output Characteristics

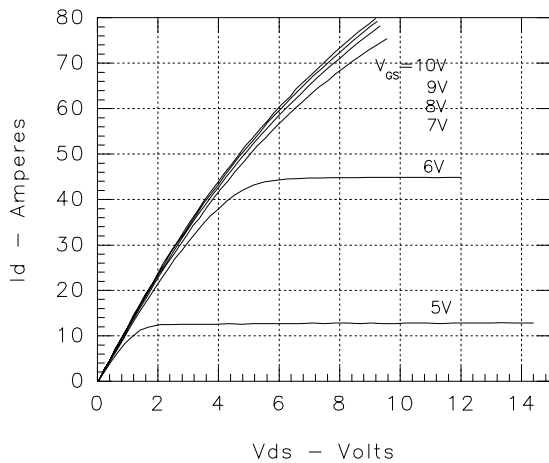


Fig. 2. Input Admittance

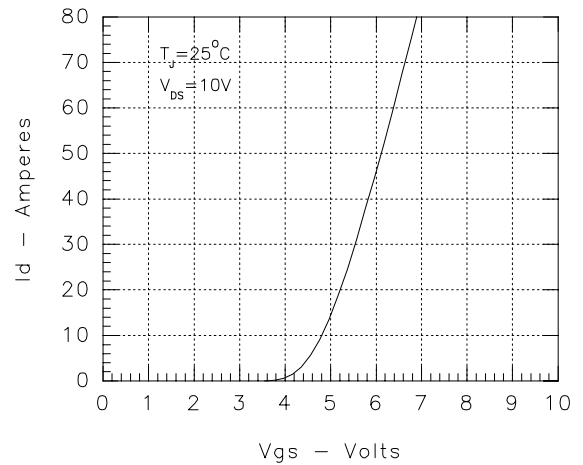


Fig. 3. Rds(on) vs. Drain Current

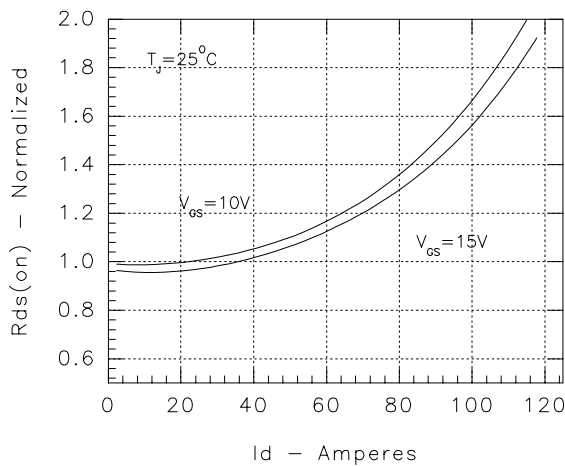


Fig. 4. Temperature Dependence of Drain to Source Resistance

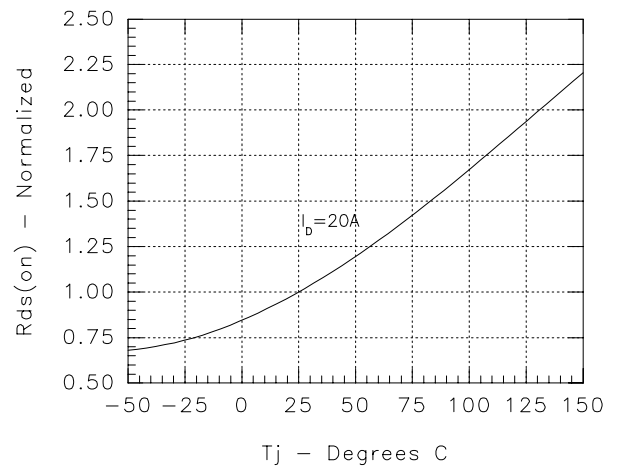


Fig. 5. Drain Current vs. Case Temperature

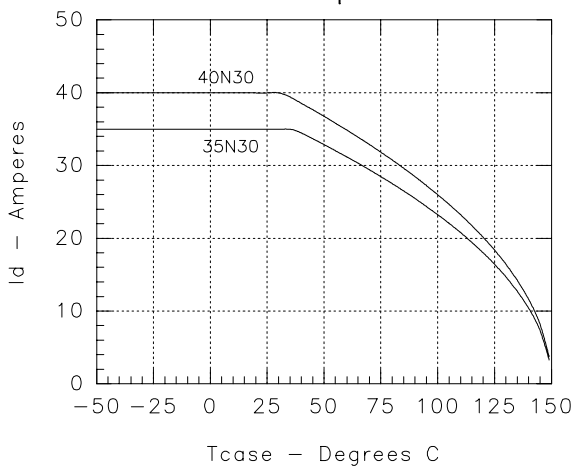


Fig. 6. Temperature Dependence of Breakdown Voltage and Threshold Voltage

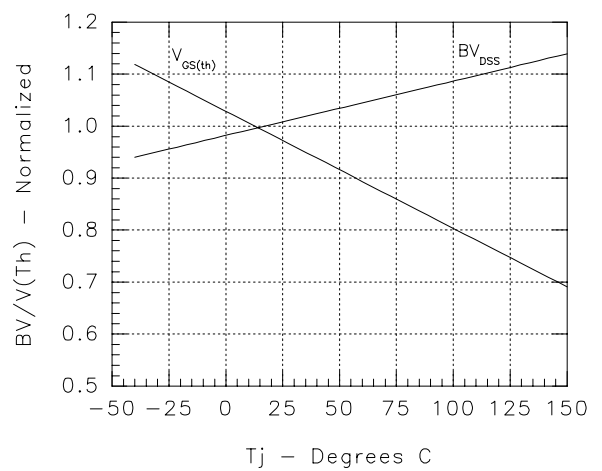


Fig.7 Gate Charge Characteristic Curve

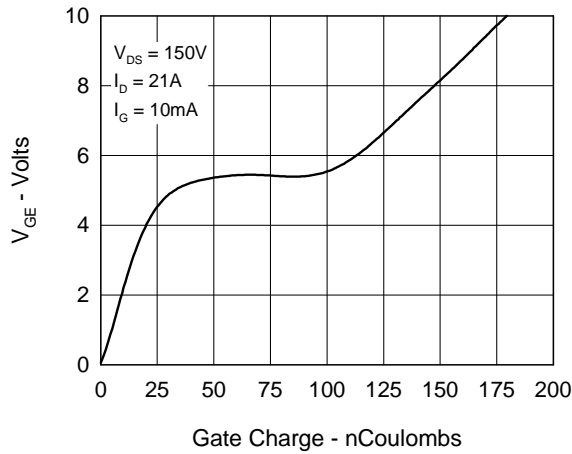


Fig.8 Forward Bias Safe Operating Area

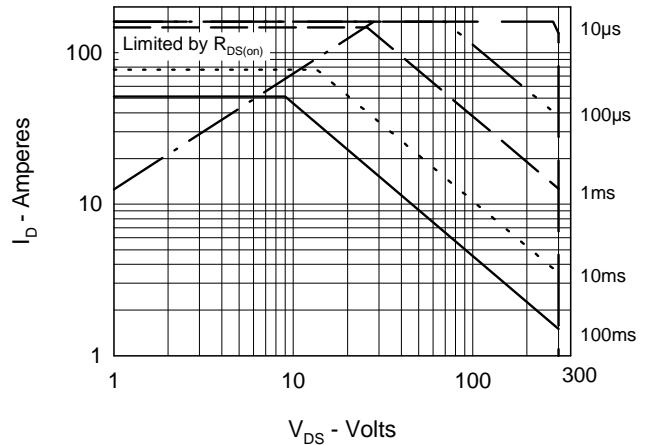


Fig.9 Capacitance Curves

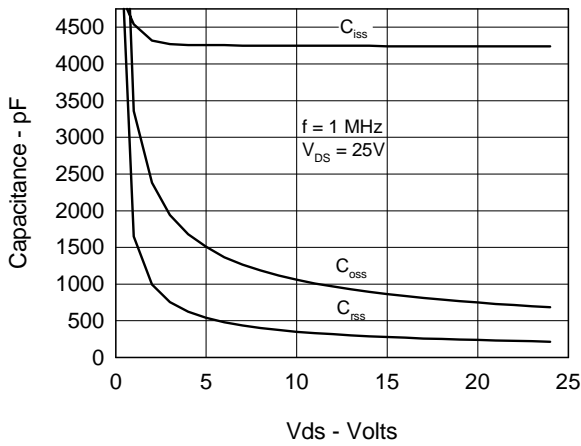


Fig.10 Source Current vs. Source

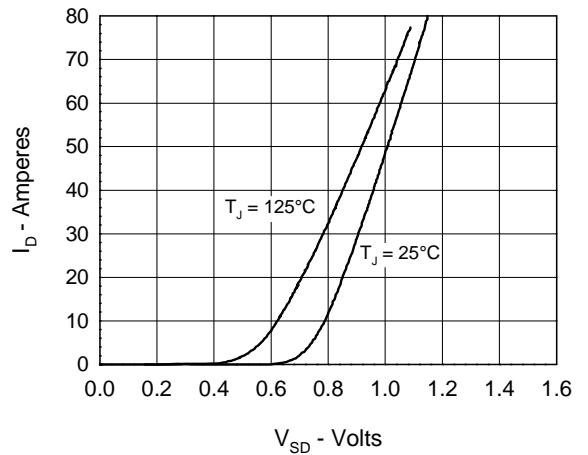
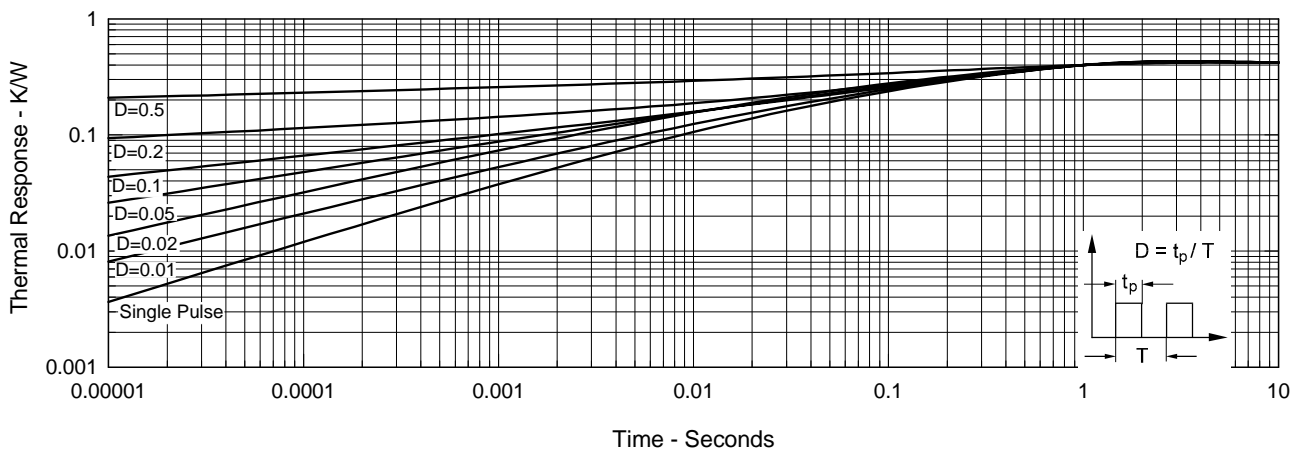


Fig.11 Transient Thermal Impedance





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