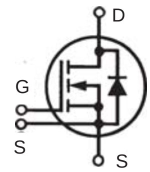
IXYS

HiPerFET™ Power MOSFETs Single Die MOSFET

IXFN 340N07

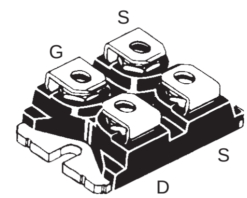
N-Channel Enhancement Mode
Avalanche Rated, High dv/dt, Low t_{rr}



V_{DSS}	=	70	V
I_{D25}	=	340	A
$R_{DS(on)}$	=	4	mΩ
t_{rr}	≤	200	ns

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	70	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	70	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C, Chip capability	340	A
$I_{L(RMS)}$	Terminal current limit	100	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	1360	A
I_{AR}	T_C = 25°C	200	A
E_{AR}	T_C = 25°C	64	mJ
E_{AS}	T_C = 25°C	4	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \leq V_{DSS}$, $T_J \leq$ 150°C, R_G = 2 Ω	10	V/ns
P_D	T_C = 25°C	700	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
V_{ISOL}	50/60 Hz, RMS t = 1 min	2500	V~
	$I_{ISOL} \leq$ 1 mA t = 1 s	3000	V~
M_d	Mounting torque	1.5/13	Nm/lb.in.
	Terminal connection torque	1.5/13	Nm/lb.in.
Weight		30	g

miniBLOC, SOT-227 B (IXFN)
E153432



G = Gate D = Drain
S = Source

Either Source terminal at miniBLOC can be used as Main or Kelvin Source

Features

- International standard package
- miniBLOC, with Aluminium nitride isolation
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- Fast intrinsic Rectifier

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 3 mA		70			V
$V_{GH(th)}$	$V_{DS} = V_{GS}$, I_D = 8 mA		2.0		4.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$	T_J = 25°C			100	µA
	V_{GS} = 0 V	T_J = 125°C			2	mA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 100A Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				4	mΩ

Applications

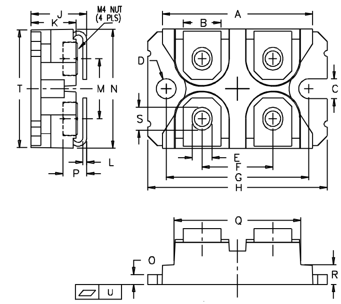
- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls
- Linear current regulators

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 60A, pulse test	80	98		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		12200		pF
C_{oss}			7100		pF
C_{rss}			3340		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 100A R_G = 1 Ω (External)		100		ns
t_r			95		ns
$t_{d(off)}$			200		ns
t_f			33		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 100A		490		nC
Q_{gs}			72		nC
Q_{gd}			266		nC
R_{thJC}				0.18	K/W
R_{thCK}			0.05		K/W

miniBLOC, SOT-227 B



M4 screws (4x) supplied

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	31.50	31.88	1.240	1.255
B	7.80	8.20	0.307	0.323
C	4.09	4.29	0.161	0.169
D	4.09	4.29	0.161	0.169
E	4.09	4.29	0.161	0.169
F	14.91	15.11	0.587	0.595
G	30.12	30.30	1.186	1.193
H	38.00	38.23	1.496	1.505
J	11.68	12.22	0.460	0.481
K	8.92	9.60	0.351	0.378
L	0.76	0.84	0.030	0.033
M	12.60	12.85	0.496	0.506
N	25.15	25.42	0.990	1.001
O	1.98	2.13	0.078	0.084
P	4.95	5.97	0.195	0.235
Q	26.54	26.90	1.045	1.059
R	3.94	4.42	0.155	0.174
S	4.72	4.85	0.186	0.191
T	24.59	25.07	0.968	0.987
U	-0.05	0.1	-0.002	0.004

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V			340	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			1360	A
V_{SD}	I_F = 100A, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.2	V
t_{rr}	I_F = 50A, -di/dt = 100 A/µs, V_R = 50V T_J = 25°C		100	200	ns
Q_{RM}			1.4		µC
I_{RM}			8		A

Fig. 1. Output Characteristics @ 25 Deg. C

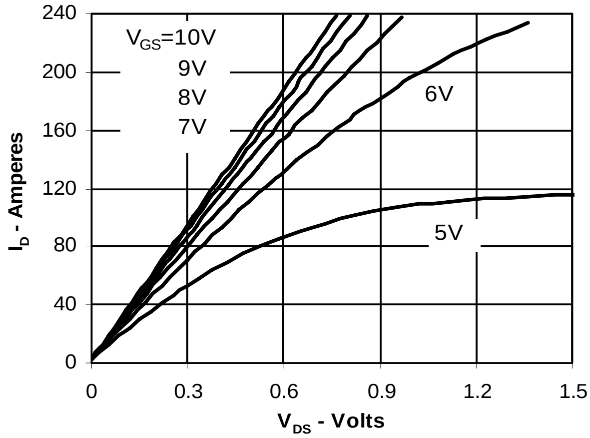


Fig. 2. Output Characteristics @ 125 Deg. C

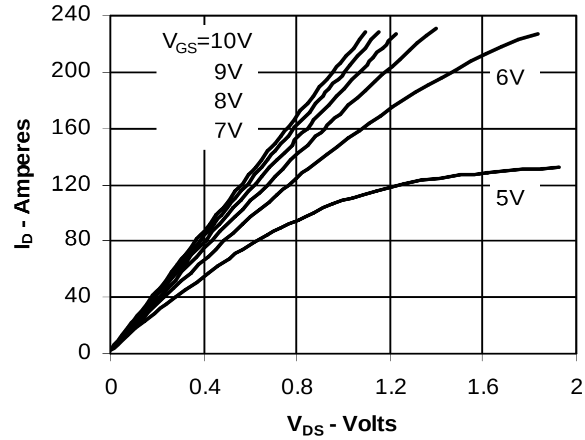


Fig. 3. Temperature Dependence of $R_{DS(ON)}$

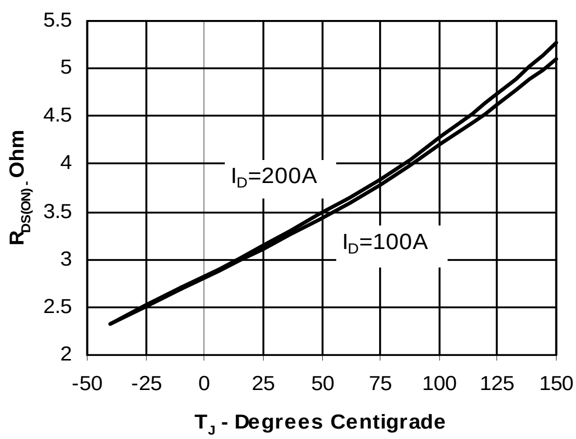


Fig. 4. $R_{DS(ON)}$ Normalized to $I_{L(RMS)}$ Value vs. Junction Temperature

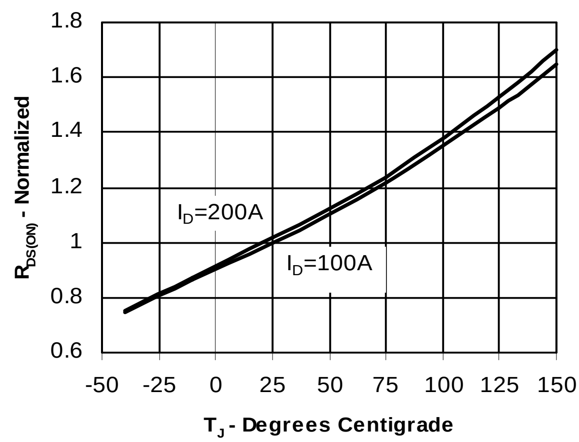


Fig. 5. $R_{DS(ON)}$ Normalized to $I_{L(RMS)}$ Value vs. I_D

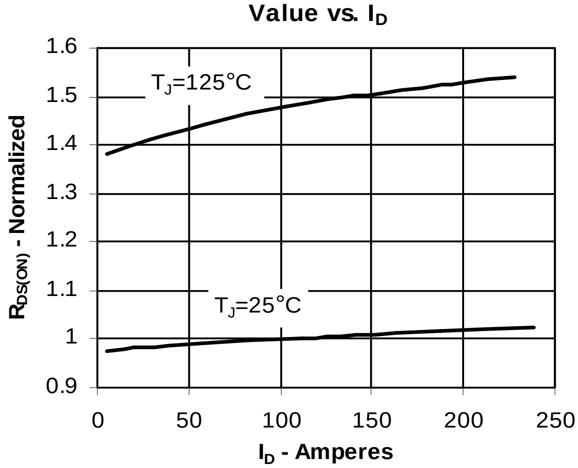


Fig. 6. Temperature dependence of Breakdown & Threshold Voltage

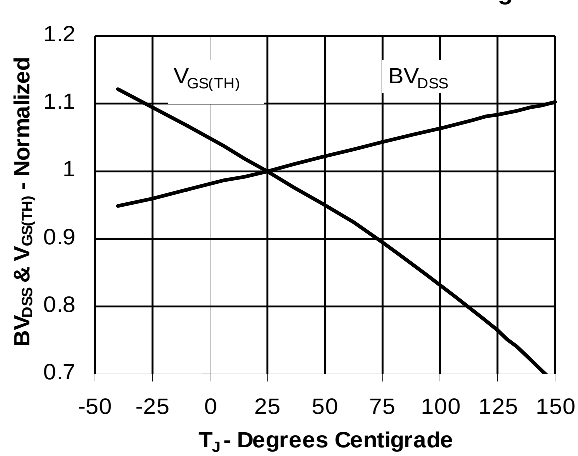


Fig. 7. Input Admittance

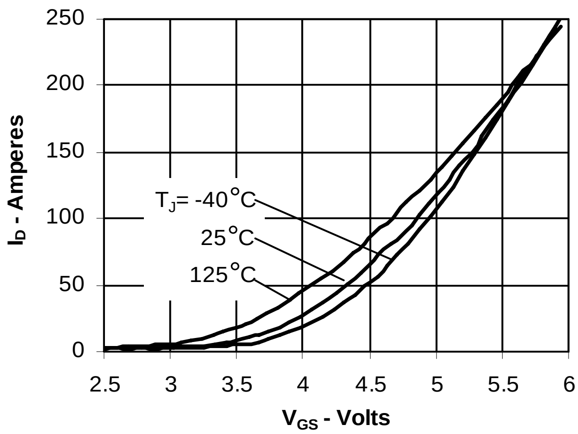


Fig. 8. Transconductance

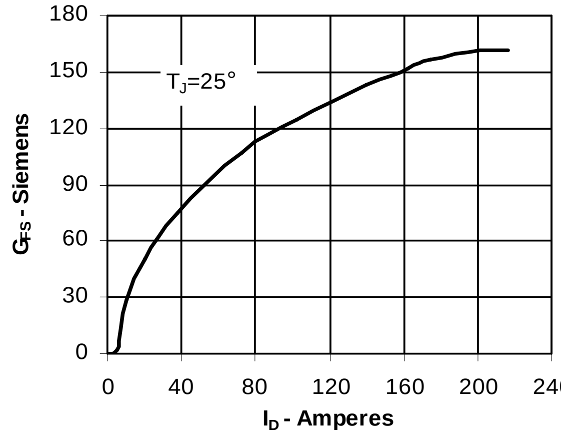


Fig. 9. Source Current vs. Source-To-Drain Voltage

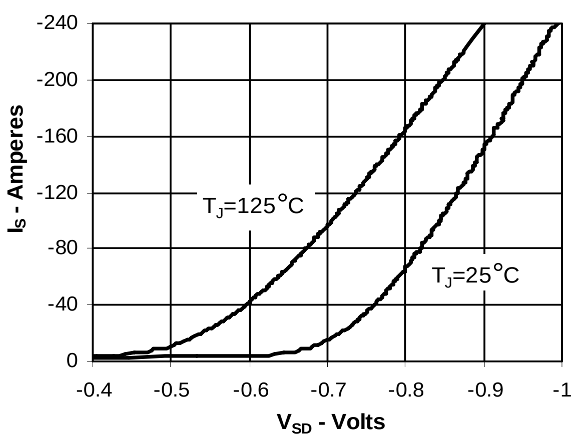


Fig. 10. Gate Charge

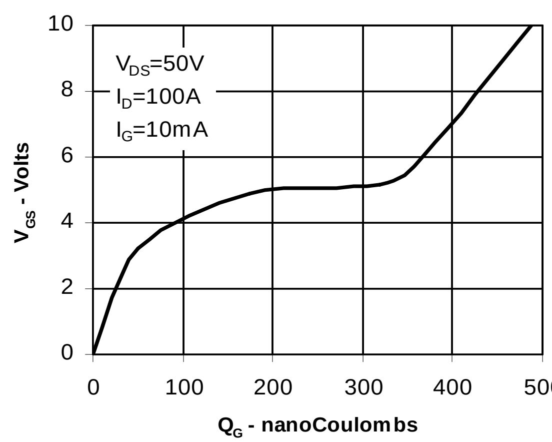


Fig. 11. Capacitance

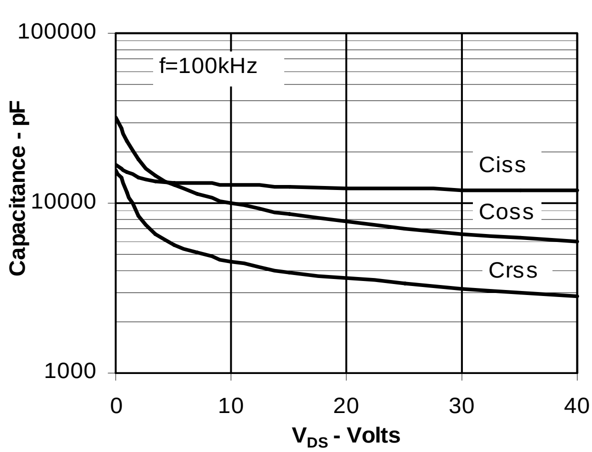


Fig. 12. Transient Thermal Resistance

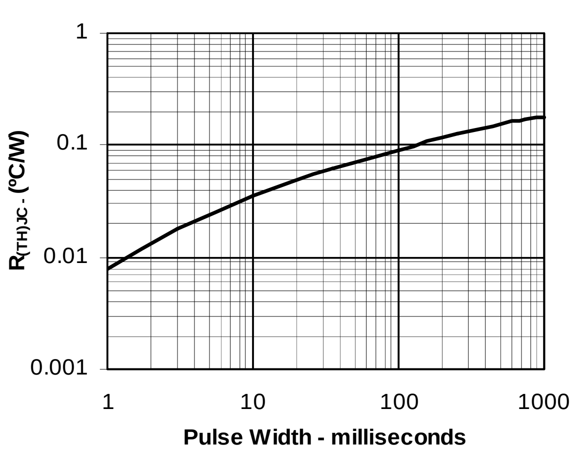


Fig. 13. Forward-Bias Safe Operating Area