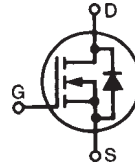


Polar™ HiPerFET™
Power MOSFET

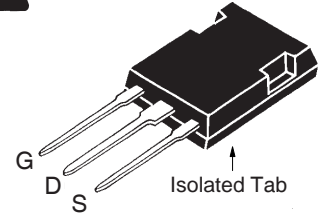
IXFR64N60P

$V_{DSS} = 600V$
 $I_{D25} = 36A$
 $R_{DS(on)} \leq 105m\Omega$
 $t_{rr} \leq 200ns$

N-Channel Enhancement Mode
Fast Intrinsic Rectifier



ISOPLUS247
E153432



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	600	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	600	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	36	A
I_{DM}	$T_C = 25^\circ C$, Pulse Width Limited by T_{JM}	150	A
I_A	$T_C = 25^\circ C$	64	A
E_{AS}	$T_C = 25^\circ C$	3.5	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$	20	V/ns
P_D	$T_C = 25^\circ C$	320	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	Plastic Body for 10s	260	$^\circ C$
V_{ISOL}	50/60 Hz, 1 Minute	2500	V~
F_C	Mounting Force	20..120/4.5..27	N/lb
Weight		5	g

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- Low Intrinsic Gate Resistance
- 2500V~ Electrical Isolation
- Dynamic dv/dt Rating
- Avalanche Rated
- Fast Intrinsic Rectifier
- Low Q_G
- Low $R_{DS(on)}$
- Low Drain-to-Tab Capacitance
- Low Package Inductance

Advantages

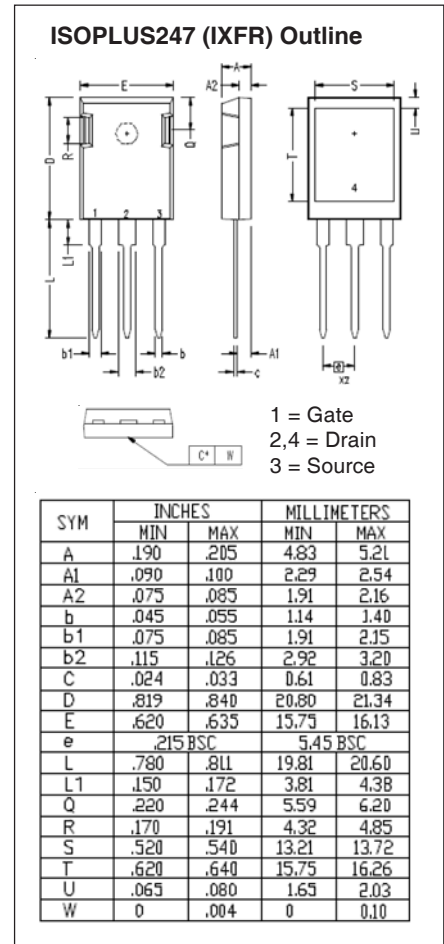
- High Power Density
- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- Uninterrupted Power Supplies
- AC Motor Drives
- High Speed Power Switching Applications

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 3mA$	600		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8mA$	3.0		5.0 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			25 μA 1 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 32A$, Note 1			105 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 20\text{V}, I_D = 32\text{A}$, Note 1	40	63	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		12	nF
C_{oss}			1150	pF
C_{rss}			80	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 32\text{A}$ $R_G = 1\Omega$ (External)		28	ns
t_r			23	ns
$t_{d(off)}$			79	ns
t_f			24	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 32\text{A}$		200	nC
Q_{gs}			70	nC
Q_{gd}			68	nC
R_{thJC}				0.39°C/W
R_{thCS}		0.15		$^\circ\text{C/W}$



Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			64 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			256 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 25\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			200 ns
Q_{RM}			0.6	μC
I_{RM}			6.0	A

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

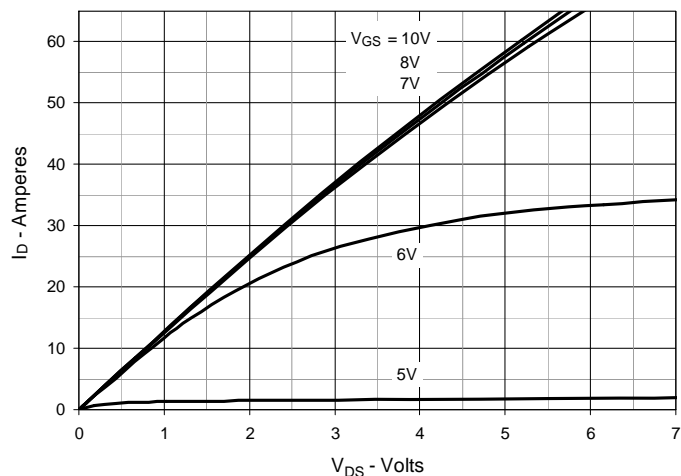
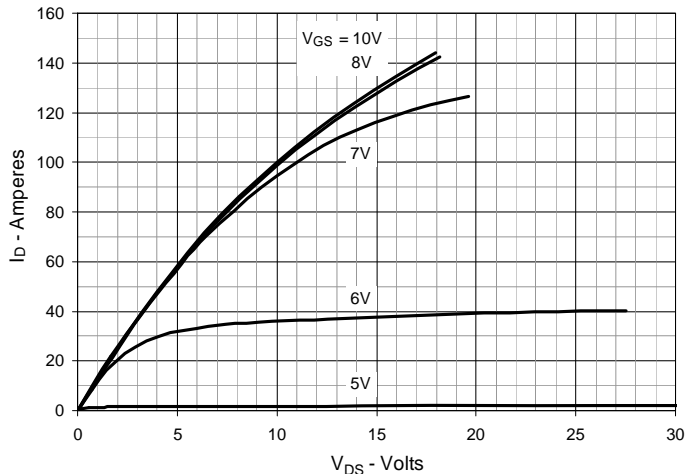
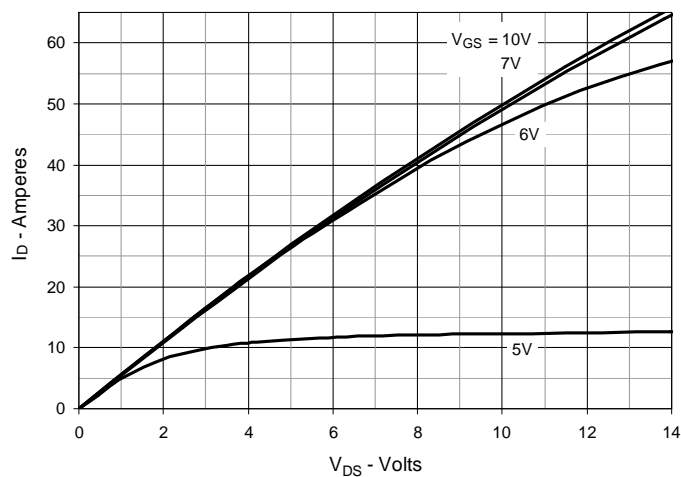
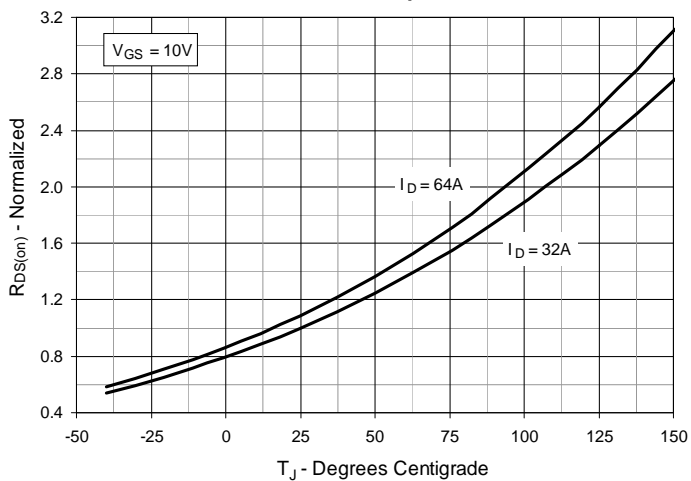
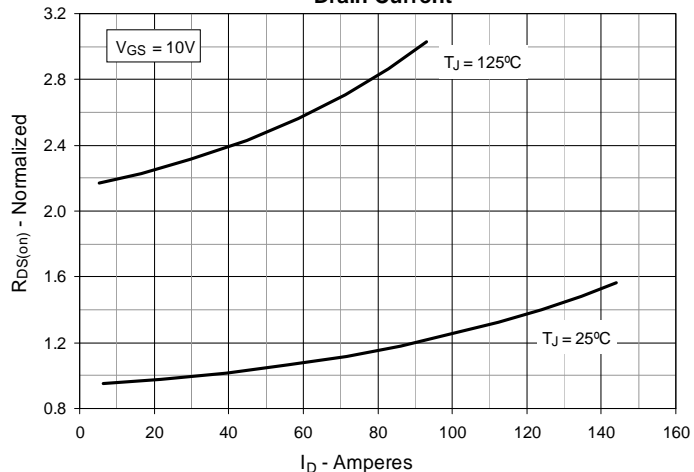
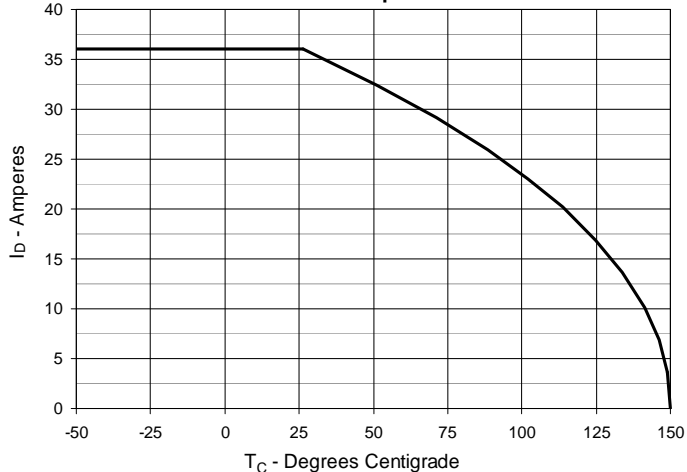
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 32\text{A}$ vs. Junction Temperature

Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 32\text{A}$ vs. Drain Current

Fig. 6. Maximum Drain Current vs. Case Temperature


Fig. 7. Input Admittance

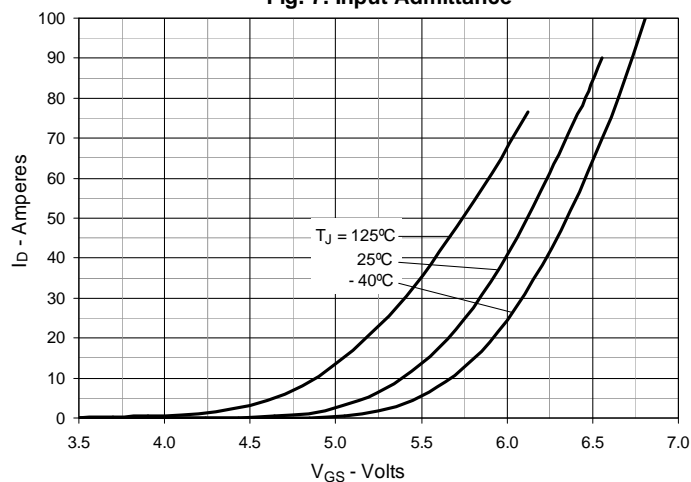


Fig. 8. Transconductance

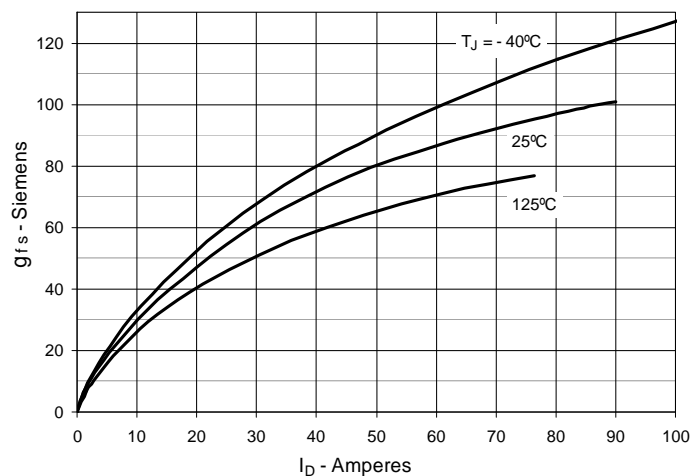


Fig. 9. Forward Voltage Drop of Intrinsic Diode

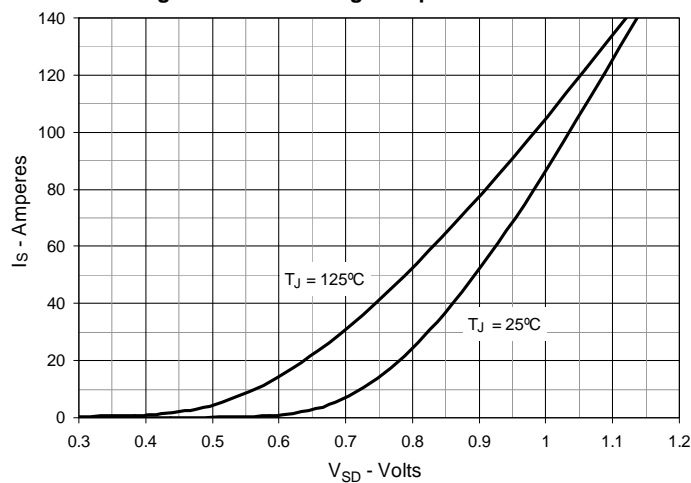


Fig. 7. Gate Charge

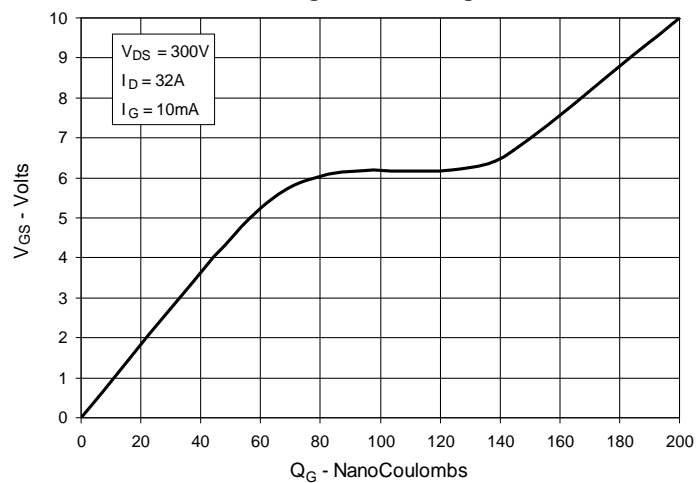


Fig. 11. Capacitance

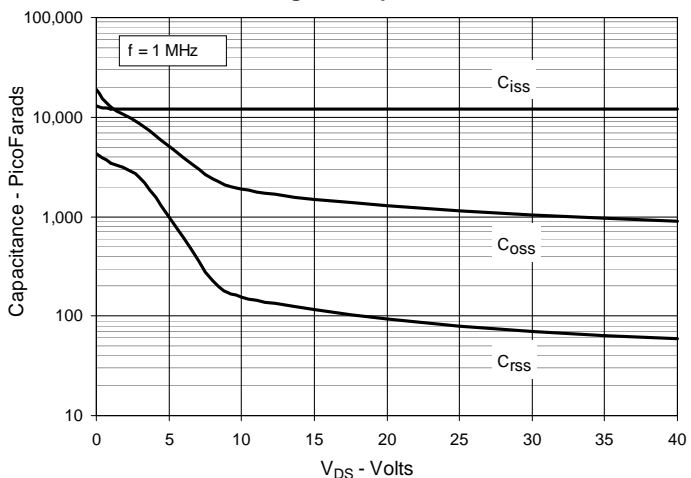


Fig. 12. Forward-Bias Safe Operating Area

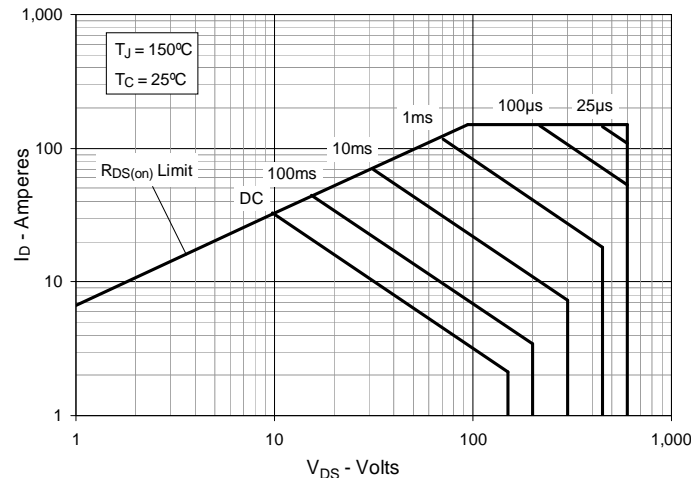
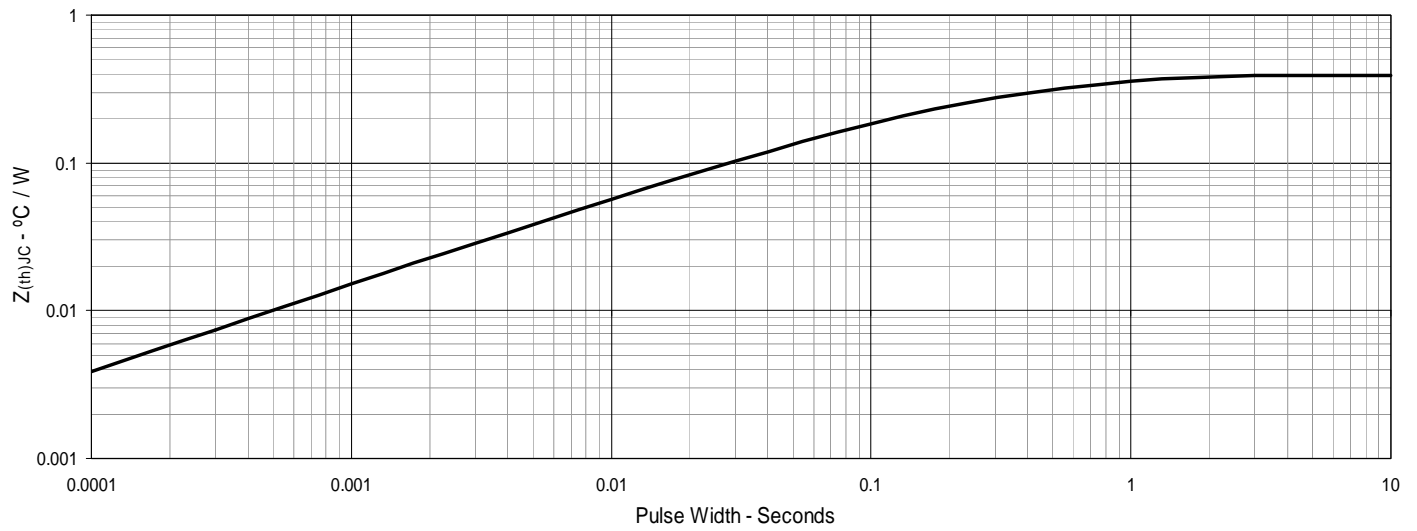


Fig. 13. Maximum Transient Thermal Impedance





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