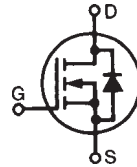


**Linear™ Power MOSFET
w/ Extended FBSOA**

**IXTK17N120L
IXTX17N120L**

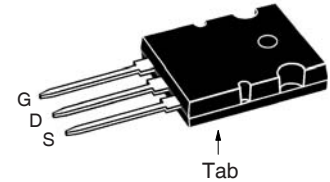
V_{DSS} = 1200V
I_{D25} = 17A
R_{DS(on)} ≤ 900mΩ

N-Channel Enhancement Mode
 Avalanche Rated
 Guaranteed FBSOA

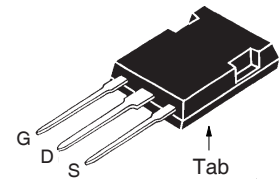


Symbol	Test Conditions	Maximum Ratings	
V _{DSS}	T _J = 25°C to 150°C	1200	V
V _{DGR}	T _J = 25°C to 150°C, R _{GS} = 1MΩ	1200	V
V _{GSS}	Continuous	±30	V
V _{GSM}	Transient	±40	V
I _{D25}	T _C = 25°C	17	A
I _{DM}	T _C = 25°C, pulse width limited by T _{JM}	34	A
I _A	T _C = 25°C	8.5	A
E _{AS}	T _C = 25°C	2.5	J
P _D	T _C = 25°C	700	W
T _J		-55...+150	°C
T _{JM}		150	°C
T _{stg}		-55...+150	°C
T _L	1.6mm (0.063 in.) from case for 10s	300	°C
T _{SOLD}	Plastic body for 10s	260	°C
M _d	Mounting torque (IXTK)	1.13/10	Nm/lb.in.
F _C	Mounting Force (IXTX)	20..120 / 4.5..27	N/lb.
Weight	TO-264	10	g
	PLUS247	6	g

TO-264 (IXTK)



PLUS247 (IXTX)



G = Gate D = Drain
 S = Source Tab = Drain

Features

- Designed for Linear Operations
- Guaranteed FBSOA at 60°C
- Avalanche Rated
- Low R_{DS(on)} HDMOS™ Process
- Molding Epoxies Meet UL94 V-0 Flammability Classification

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Programmable Loads
- Current Regulators
- DC-DC Convertors
- Battery Chargers
- DC Choppers
- Temperature and Lighting Controls

Symbol	Test Conditions (T _J = 25°C, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV _{DSS}	V _{GS} = 0V, I _D = 1mA	1200		V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	3.0		6.0 V
I _{GSS}	V _{GS} = ±30V, V _{DS} = 0V			±200 nA
I _{DSS}	V _{DS} = V _{DSS} , V _{GS} = 0V T _J = 125°C			50 μA 2 mA
R _{DS(on)}	V _{GS} = 20V, I _D = 0.5 • I _{DSS} , Note 1			900 mΩ

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values			
		Min.	Typ.	Max.	
g_{fs}	$V_{DS} = 20\text{V}$, $I_D = 0.5 \cdot I_{DSS}$, Note 1	3.5	5.0	6.5	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		8300		pF
C_{oss}			520		pF
C_{rss}			90		pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 15\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{DSS}$ $R_G = 2\Omega$ (External)		42		ns
t_r			31		ns
$t_{d(off)}$			110		ns
t_f			83		ns
$Q_{g(on)}$		$V_{GS} = 15\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{DSS}$		155	
Q_{gs}			41		nC
Q_{gd}			60		nC
R_{thJC}				0.18	$^\circ\text{C/W}$
R_{thCS}			0.15		$^\circ\text{C/W}$

Safe Operating Area Specification

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
SOA	$V_{DS} = 800\text{V}$, $I_D = 0.3\text{A}$, $T_C = 60^\circ\text{C}$, $t_p = 3\text{s}$	240		W

Source-Drain Diode

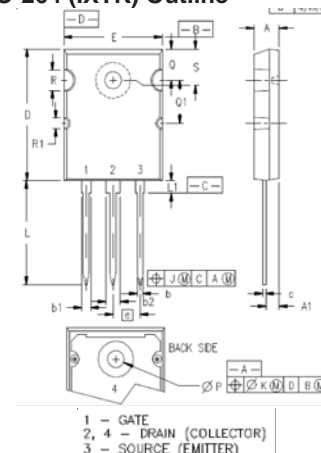
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values			
		Min.	Typ.	Max.	
I_S	$V_{GS} = 0\text{V}$			17	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			50	A
V_{SD}	$I_F = 17\text{A}$, $V_{GS} = 0\text{V}$, Note 1			1.5	V
t_{rr}	$I_F = I_S$, $-di/dt = 100\text{A}/\mu\text{s}$, $V_R = 100\text{V}$		1830		ns

Note: 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

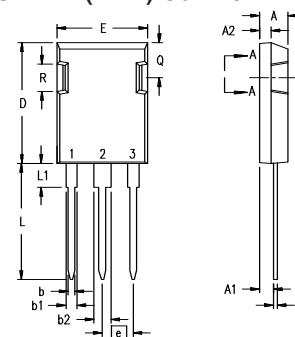
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338 B2
4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

TO-264 (IXTK) Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215 BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
Q	.122	.138	3.10	3.51
Q1	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
Q1	.155	.187	3.94	4.75
Q1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

PLUS 247™ (IXTX) Outline



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)
4 - Drain (Collector)

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.83	5.21	.190	.205
A ₁	2.29	2.54	.090	.100
A ₂	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b ₁	1.91	2.13	.075	.084
b ₂	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

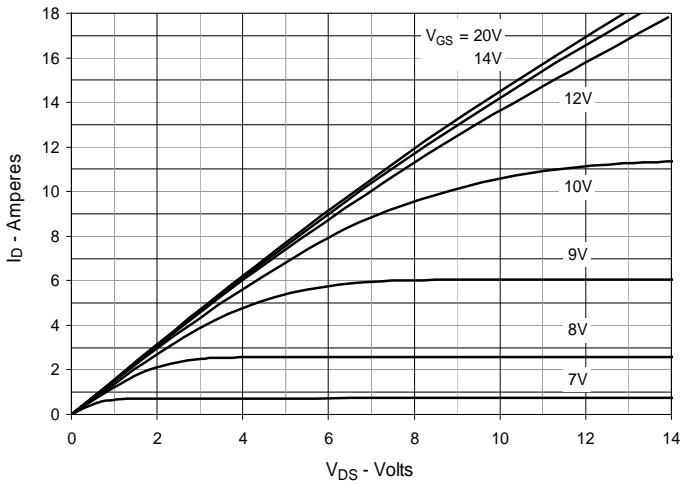


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

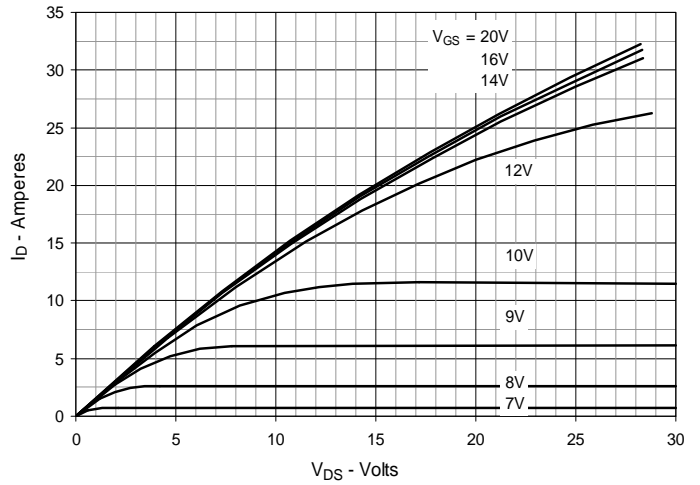


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

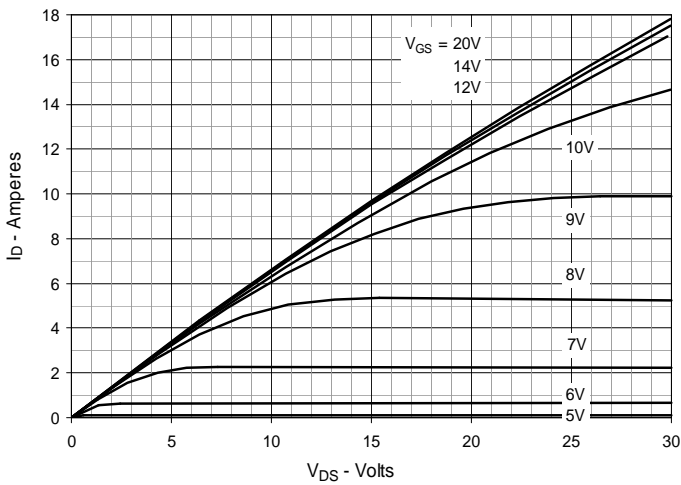


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 8.5\text{A}$ Value vs. Junction Temperature

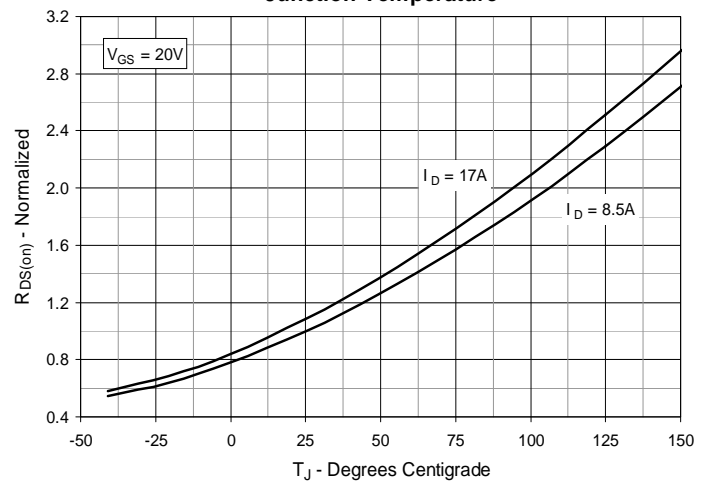


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 8.5\text{A}$ Value vs. Drain Current

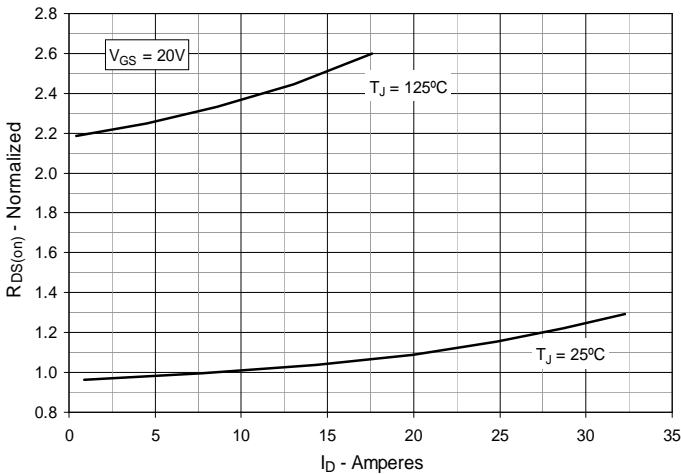


Fig. 6. Maximum Drain Current vs. Case Temperature

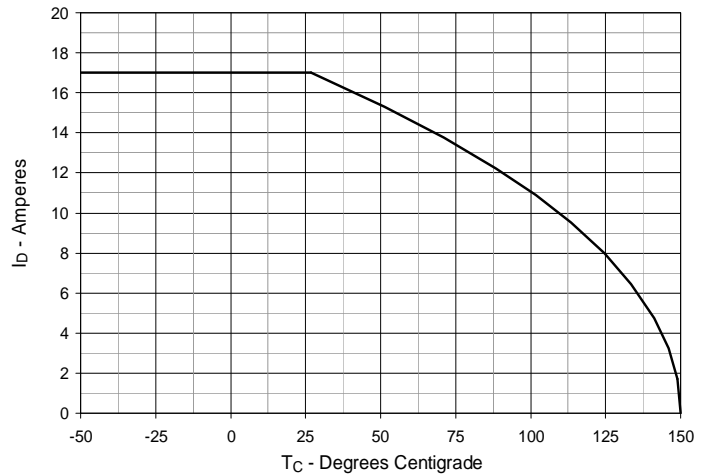


Fig. 7. Input Admittance

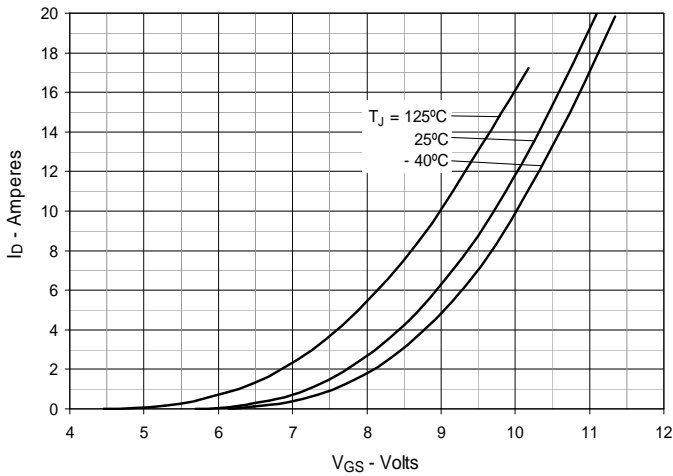


Fig. 8. Transconductance

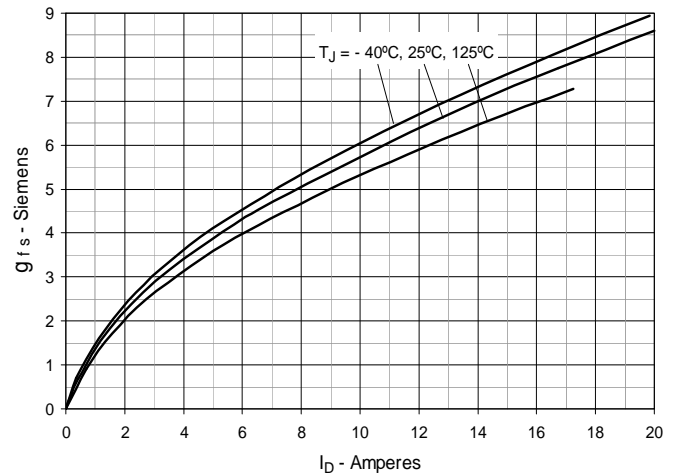


Fig. 9. Forward Voltage Drop of Intrinsic Diode

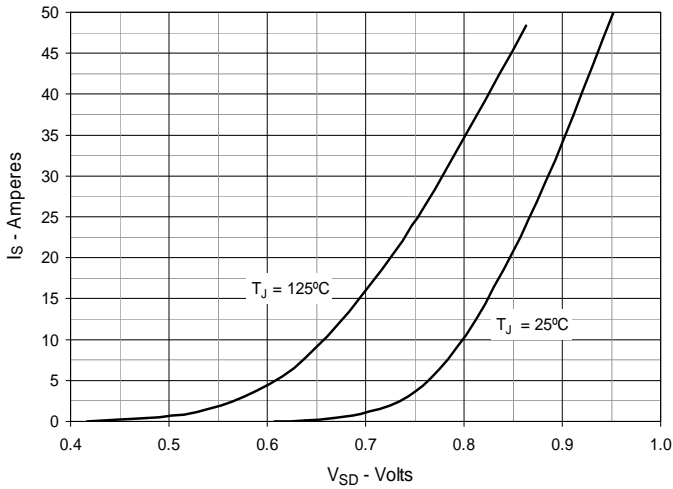


Fig. 10. Gate Charge

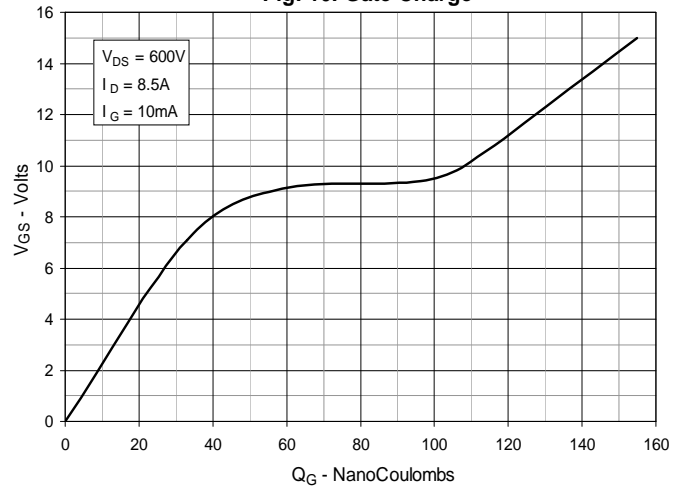


Fig. 11. Capacitance

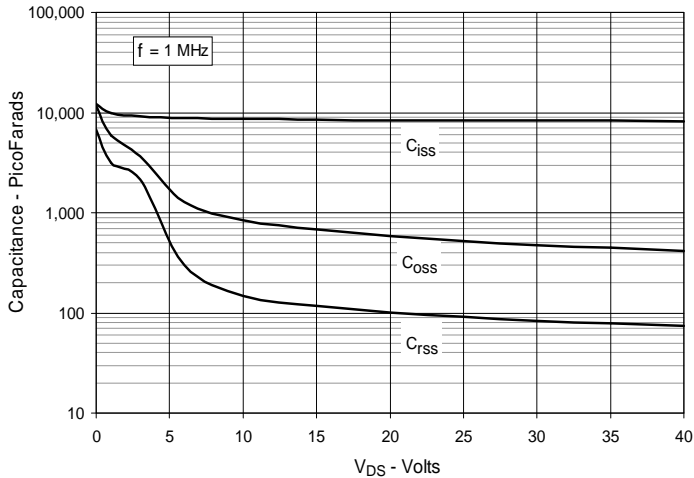
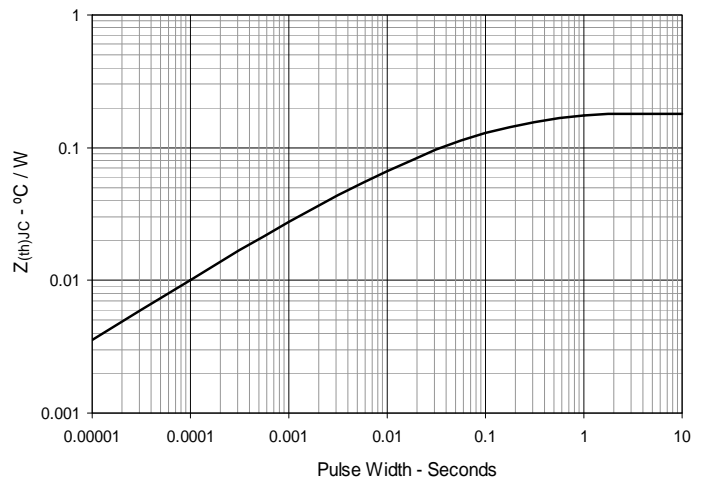
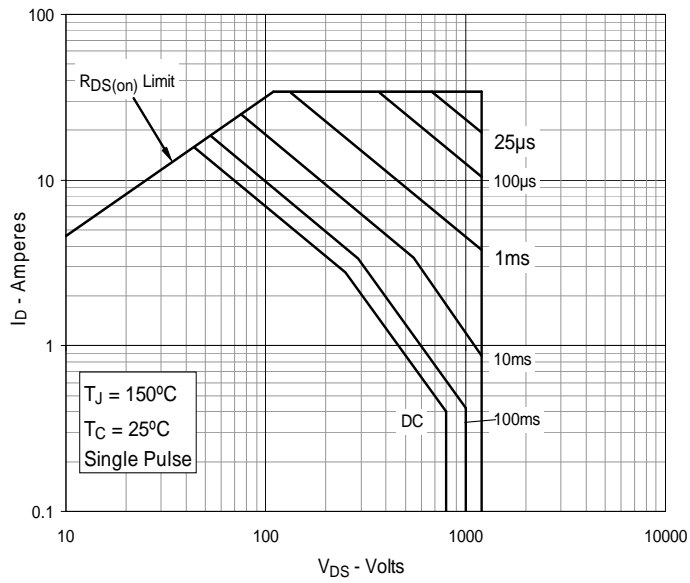


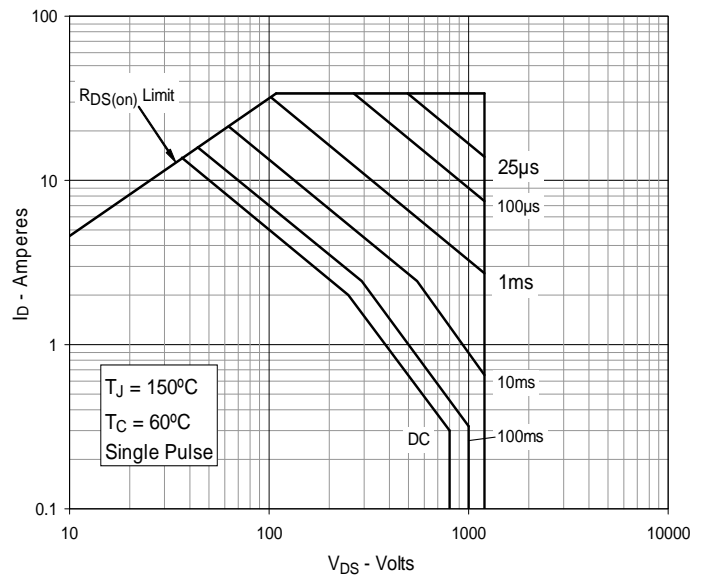
Fig. 12. Maximum Transient Thermal Impedance



**Fig. 13. Forward-Bias Safe Operating Area
@ $T_C = 25^\circ\text{C}$**



**Fig. 14. Forward-Bias Safe Operating Area
@ $T_C = 60^\circ\text{C}$**





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