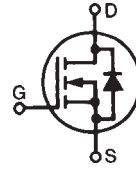


# MegaMOS™ FET

IXTH / IXTM 67N10  
IXTH / IXTM 75N10  
IXTT 75N10

$V_{DSS}$	$I_{D25}$	$R_{DS(on)}$
100 V	67 A	25 mΩ
100 V	75 A	20 mΩ

N-Channel Enhancement Mode



Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	100	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ ; $R_{GS} = 1\text{ M}\Omega$	100	V
$V_{GS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$	67N10 75N10	67 75 A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , pulse width limited by $T_{JM}$	67N10 75N10	268 300 A
$P_D$	$T_C = 25^\circ\text{C}$	300	W
$T_J$		-55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		-55 ... +150	$^\circ\text{C}$
$M_d$	Mounting torque	1.13/10	Nm/lb.in.
<b>Weight</b>		TO-204	18 g
		TO-247	6 g
		TO-268	5 g
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		10	$^\circ\text{C}$

TO-247 AD (IXTH)

TO-204 AE (IXTM)

TO-268 (IXTT)

G = Gate,  
S = Source,

D = Drain,  
TAB = Drain

### Features

- International standard packages
- Low  $R_{DS(on)}$  HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic Rectifier

### Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls
- Low voltage relays

### Advantages

- Easy to mount with 1 screw (TO-247) (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		min.	typ.	max.
$V_{DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\ \mu\text{A}$	100		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 4\text{ mA}$	2.0		V
$I_{GSS}$	$V_{GS} = \pm 20\text{ V}_{DC}$ , $V_{DS} = 0$			$\pm 100\text{ nA}$
$I_{DSS}$	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		250 $\mu\text{A}$
		$T_J = 125^\circ\text{C}$		1 mA
$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 0.5 I_{D25}$  Pulse test, $t \leq 300\ \mu\text{s}$ , duty cycle $d \leq 2\%$	67N10		0.025 $\Omega$
		75N10		0.020 $\Omega$

IXYS reserves the right to change limits, test conditions, and dimensions.

DS91533F(9/03)

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)			
		min.	typ.	max.	
$g_{fs}$	$V_{DS} = 10\text{ V}; I_D = I_{D25}$ , pulse test	25	30	S	
$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		4500	pF	
$C_{oss}$			1300	pF	
$C_{rss}$			550	pF	
$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 I_{D25}$ $R_G = 2\ \Omega$ , (External)		40	60	ns
$t_r$			60	110	ns
$t_{d(off)}$			100	140	ns
$t_f$			30	60	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 I_{D25}$		180	260	nC
$Q_{gs}$			30	70	nC
$Q_{gd}$			90	160	nC
$R_{thJC}$	(TO-204, TO-247)			0.42	K/W
$R_{thCK}$			0.25		K/W

**Source-Drain Diode**

Symbol	Test Conditions	Characteristic Values ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)			
		min.	typ.	max.	
$I_S$	$V_{GS} = 0\text{ V}$	67N10 75N10		67 75	A A
$I_{SM}$	Repetitive; pulse width limited by $T_{JM}$	67N10 75N10		268 300	A A
$V_{SD}$	$I_F = I_S, V_{GS} = 0\text{ V}$ , Pulse test, $t \leq 300\ \mu\text{s}$ , duty cycle $d \leq 2\%$			1.75	V
$t_{rr}$	$I_F = I_S, -di/dt = 100\text{ A}/\mu\text{s}, V_R = 100\text{ V}$		200		ns

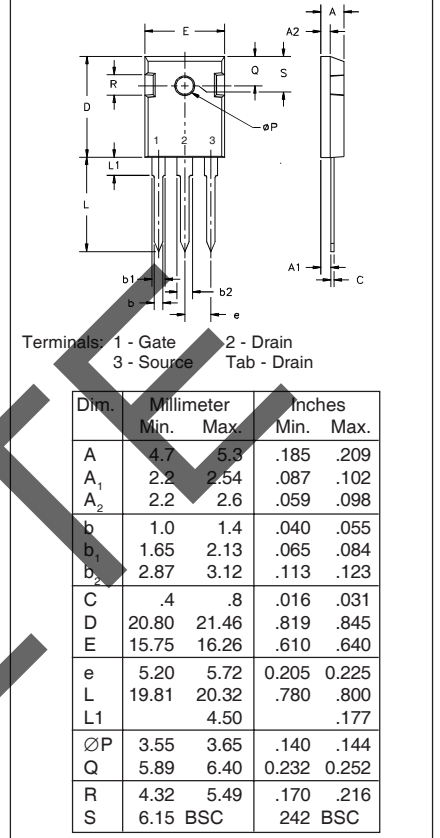
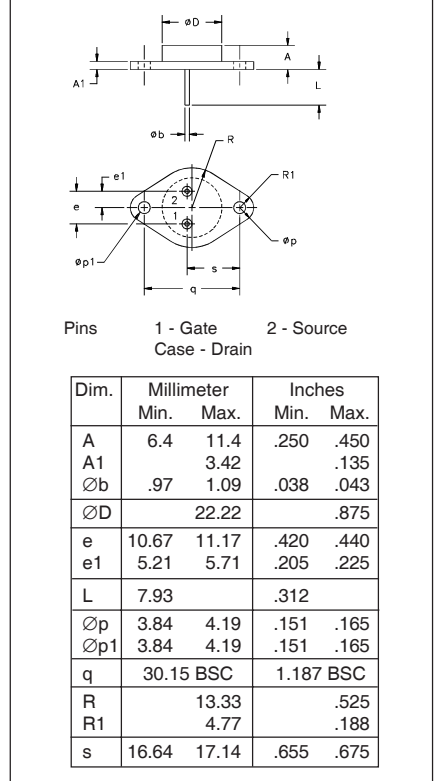
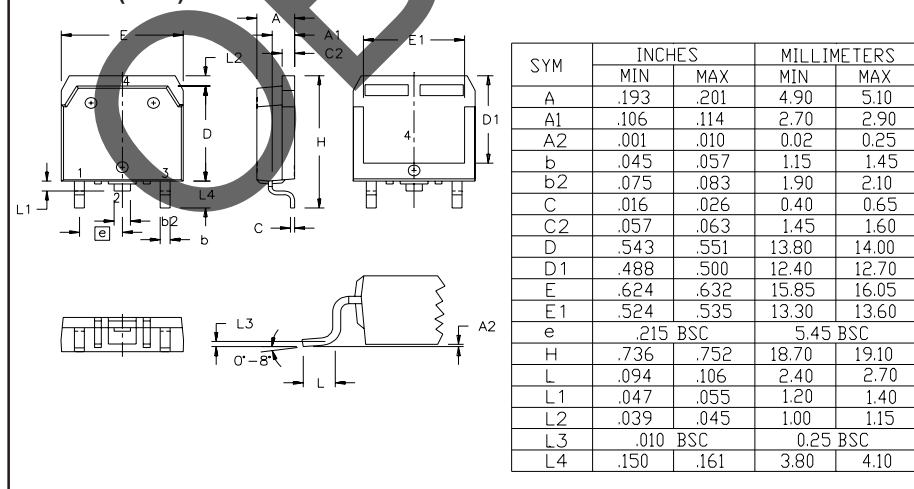
**TO-247 AD (IXTH) Outline**

**TO-204AE (IXTM) Outline**

**TO-268 (IXTT) Outline**


Fig. 1 Output Characteristics

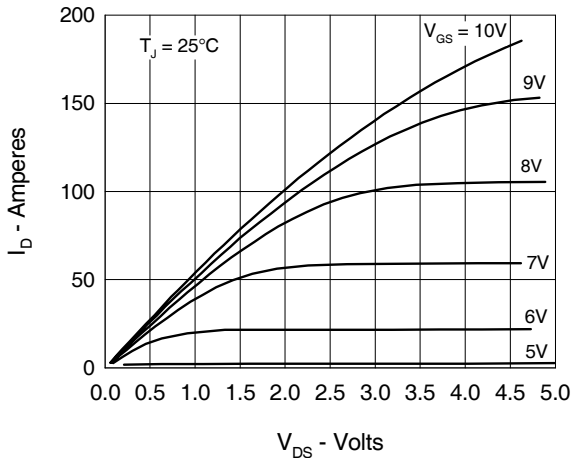


Fig. 2 Input Admittance

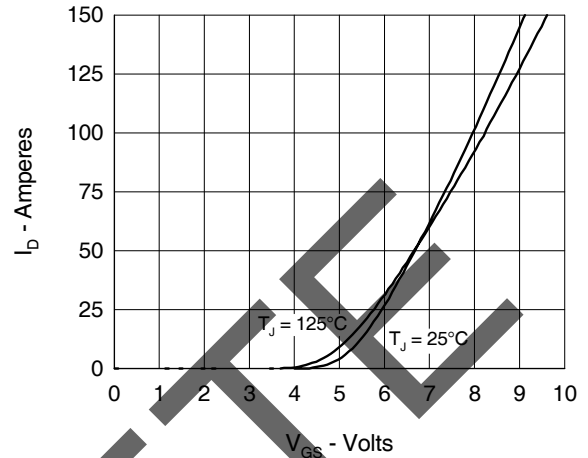


Fig. 3  $R_{DS(on)}$  vs. Drain Current

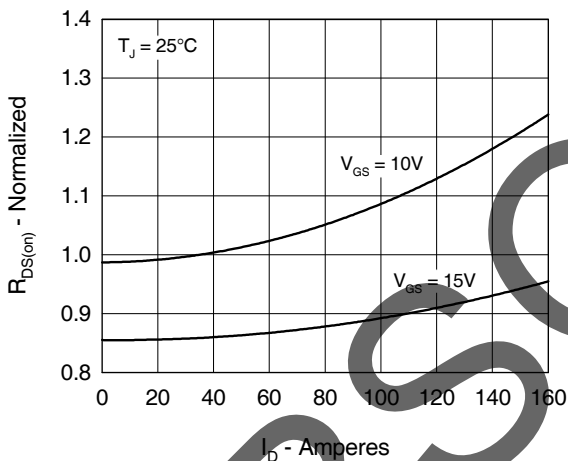


Fig. 4 Temperature Dependence of Drain to Source Resistance

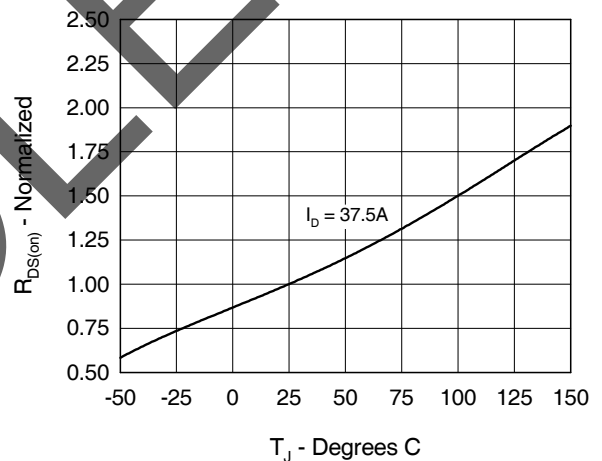


Fig. 5 Drain Current vs. Case Temperature

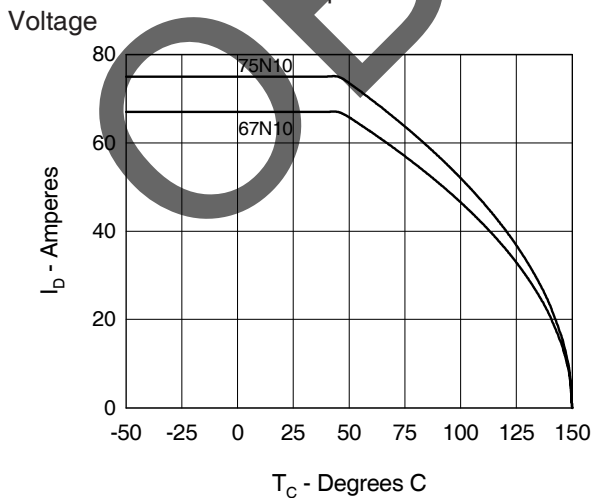


Fig. 6 Temperature Dependence of Breakdown and Threshold

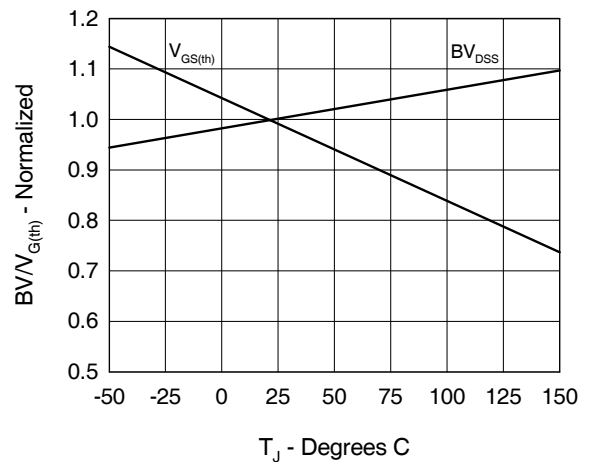


Fig.7 Gate Charge Characteristic Curve

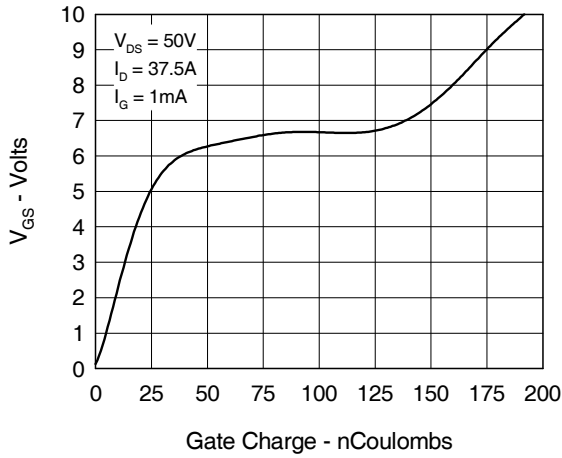


Fig.9 Capacitance Curves

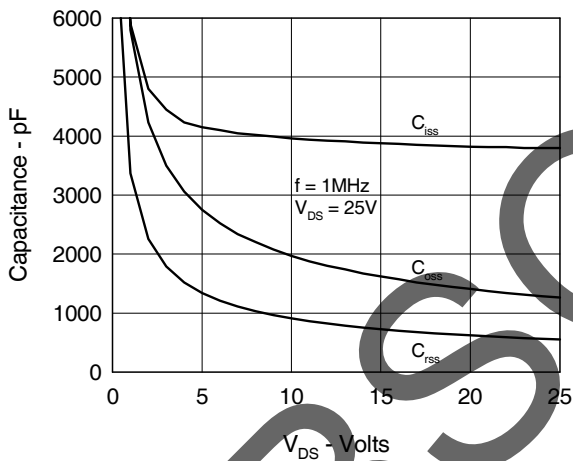


Fig.11 Transient Thermal Impedance

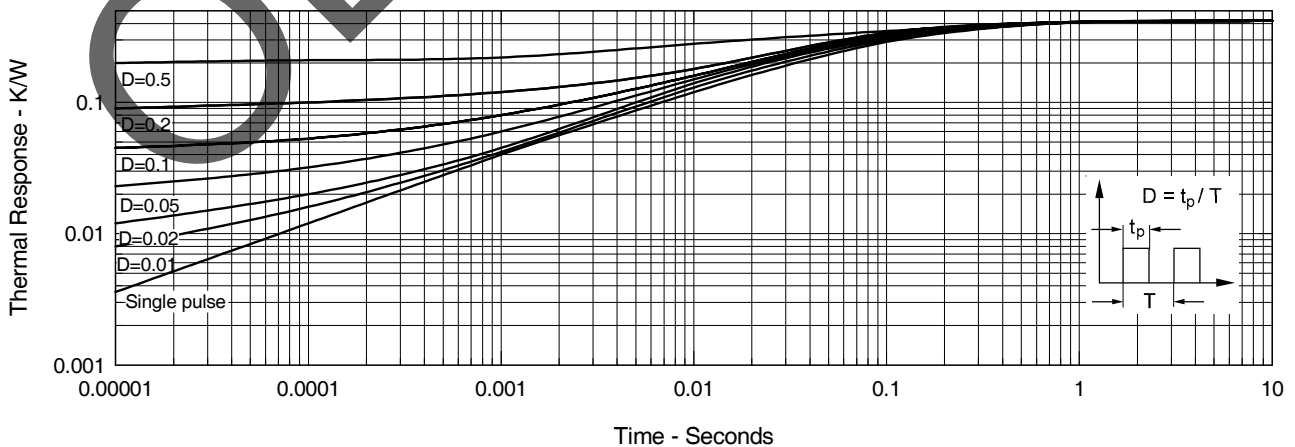


Fig.8 Forward Bias Safe Operating Area

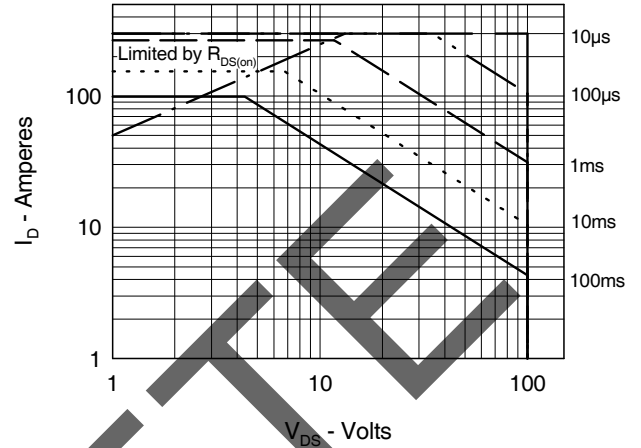
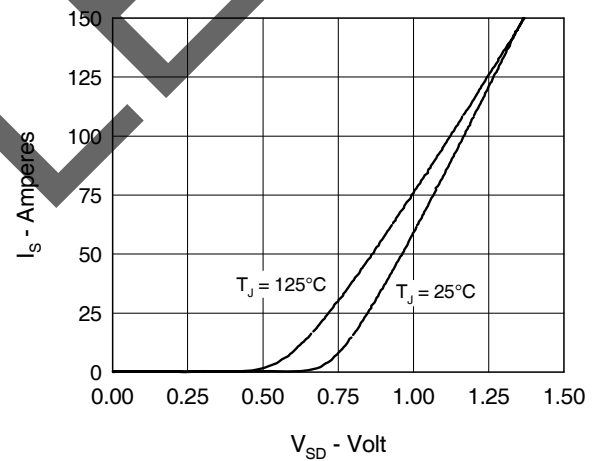


Fig.10 Source Current vs. Source to Drain Voltage





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