

# High Voltage Power MOSFET

## IXTF1N250

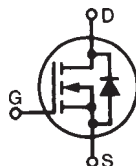
$$V_{DSS} = 2500V$$

$$I_{D25} = 1A$$

$$R_{DS(on)} \leq 40\Omega$$

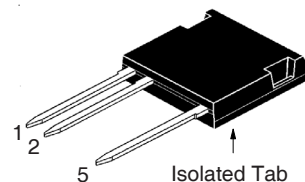
N-Channel Enhancement Mode

(Electrically Isolated Tab)



Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	2500	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ , $R_{GS} = 1M\Omega$	2500	V
$V_{GSS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$	1	A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , Pulse Width Limited by $T_{JM}$	6	A
$P_D$	$T_C = 25^\circ\text{C}$	110	W
$T_J$		- 55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		- 55 ... +150	$^\circ\text{C}$
$T_L$	1.6mm (0.062 in.) from Case for 10s	300	$^\circ\text{C}$
$T_{SOLD}$	Plastic Body for 10s	260	$^\circ\text{C}$
$M_d$	Mounting Force	20..120 / 4.5..27	Nm/lb.in.
$V_{ISOL}$	50/60Hz, 1min	2500	V~
<b>Weight</b>		5	g

### ISOPLUS i4-Pak™



1 = Gate  
2 = Source  
5 = Drain

### Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V Electrical Isolation
- Molding Epoxies meet UL 94 V-0 Flammability Classification

### Advantages

- Easy to Mount
- Space Savings
- High Power Density

### Applications

- High Voltage Power Supplies
- Capacitor Discharge
- Pulse Circuits

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0V$ , $I_D = 250\mu\text{A}$	2500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2.0		V
$I_{GSS}$	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			$\pm 100$ nA
$I_{DSS}$	$V_{DS} = 0.8 \cdot V_{DSS}$ , $V_{GS} = 0V$ Note 2, $T_J = 125^\circ\text{C}$		25	$\mu\text{A}$ $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 10V$ , $I_D = 0.5 \cdot I_{D25}$ , Note 1			40 $\Omega$

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 50\text{V}$ , $I_D = 0.5 \cdot I_{D25}$ , Note 1	1.0	1.8	mS
$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$		1660	pF
$C_{oss}$			77	pF
$C_{rss}$			23	pF
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = I_{D25}$ $R_G = 5\Omega$ (External)		69	ns
$t_r$			25	ns
$t_{d(off)}$			132	ns
$t_f$			39	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$ , $V_{DS} = 600\text{V}$ , $I_D = 0.5 \cdot I_{D25}$		41	nC
$Q_{gs}$			8	nC
$Q_{gd}$			16	nC
$R_{thJC}$			1.13	$^\circ\text{C/W}$
$R_{thCS}$		0.21		$^\circ\text{C/W}$

### Source-Drain Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$I_s$	$V_{GS} = 0\text{V}$			1.5 A
$I_{SM}$	Repetitive, pulse width limited by $T_{JM}$			6 A
$V_{SD}$	$I_F = 1\text{A}$ , $V_{GS} = 0\text{V}$ , Note 1			1.5 V
$t_{rr}$	$I_F = 1\text{A}$ , $-di/dt = 100\text{A}/\mu\text{s}$ , $V_R = 200\text{V}$		2.5	$\mu\text{s}$

- Notes
1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .
  2. Device must be heatsunk for high-temp  $I_{DSS}$  measurement to avoid thermal runaway.

**ISOPLUS i4-Pak™ (HV) Outline**

Pin 1 = Gate  
Pin 2 = Source  
Pin 3 = Drain  
Tab 4 = Isolated

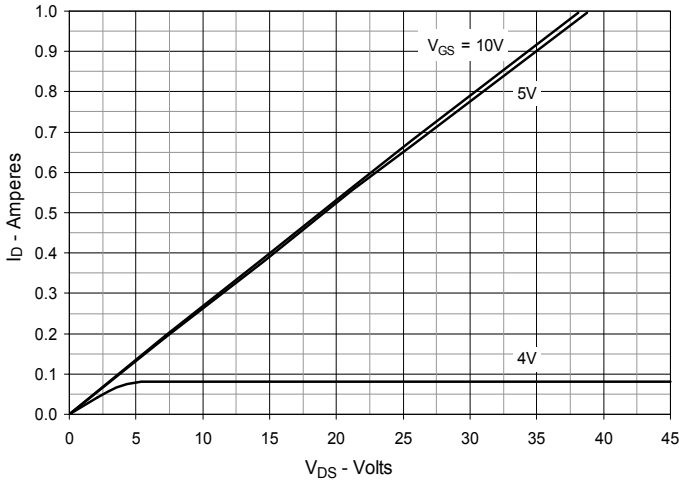
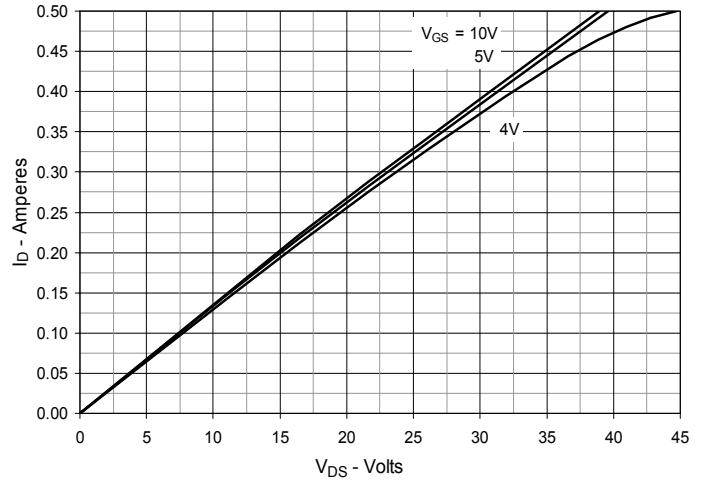
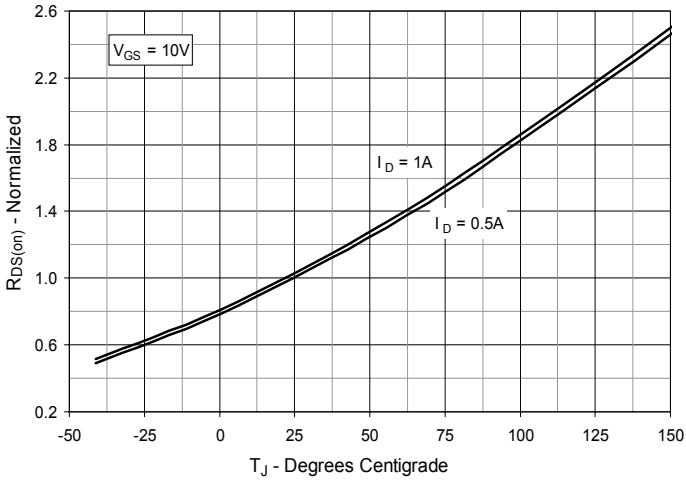
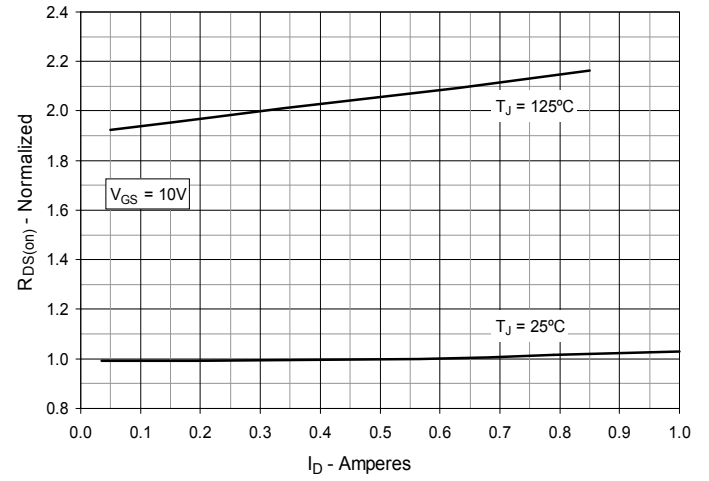
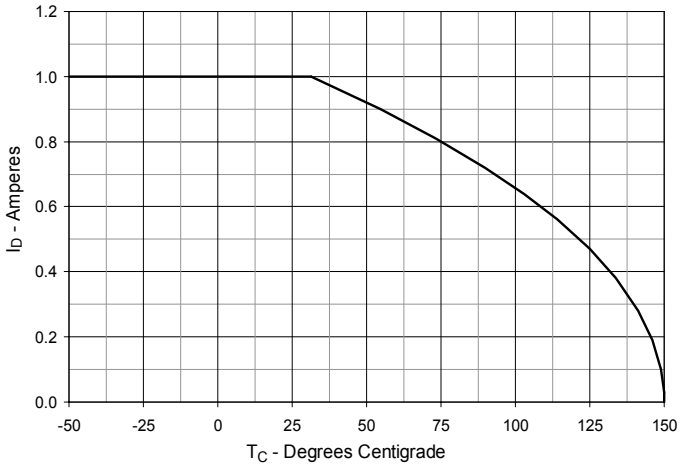
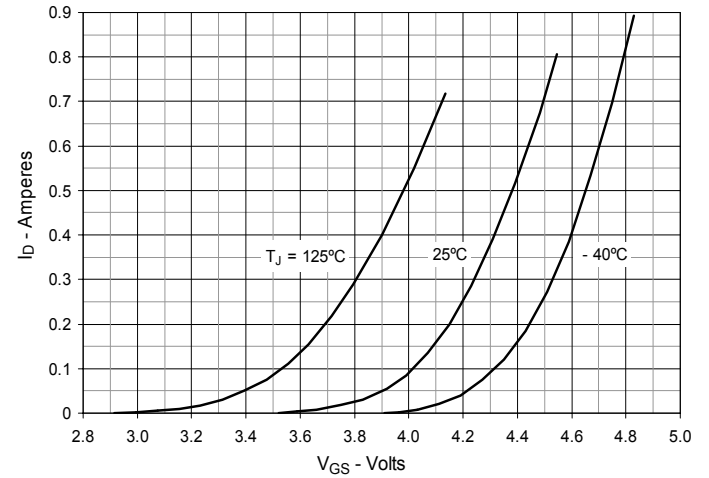
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

### ADVANCE TECHNICAL INFORMATION

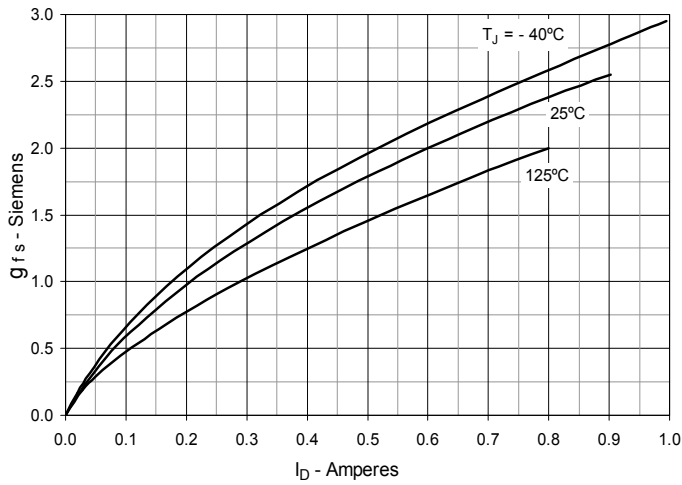
The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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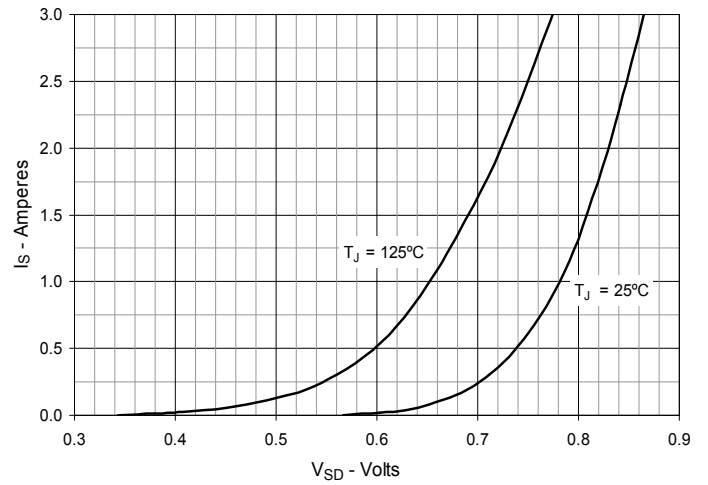
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

**Fig. 1. Output Characteristics @  $T_J = @ 25^\circ\text{C}$** 

**Fig. 2. Output Characteristics @  $T_J = 125^\circ\text{C}$** 

**Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 0.5\text{A}$  Value vs. Junction Temperature**

**Fig. 3.  $R_{DS(on)}$  Normalized to  $I_D = 0.5\text{A}$  Value vs. Drain Current**

**Fig. 5. Maximum Drain Current vs. Case Temperature**

**Fig. 6. Input Admittance**


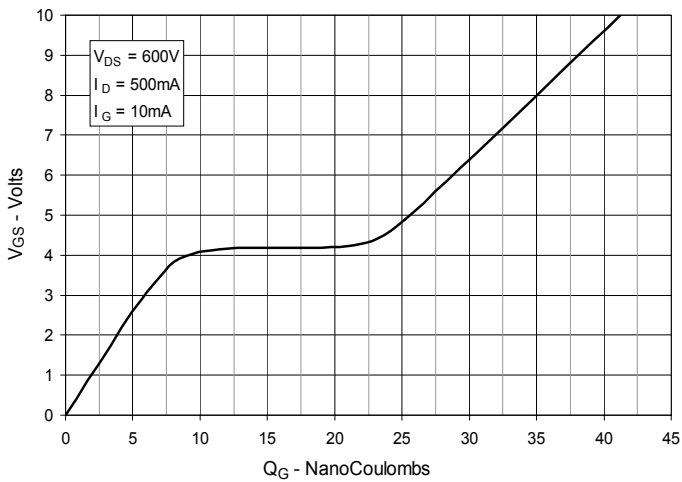
**Fig. 7. Transconductance**



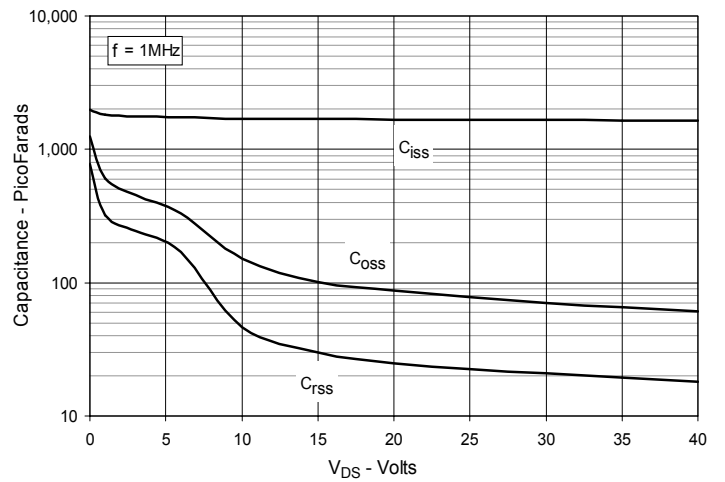
**Fig. 8. Forward Voltage Drop of Intrinsic Diode**



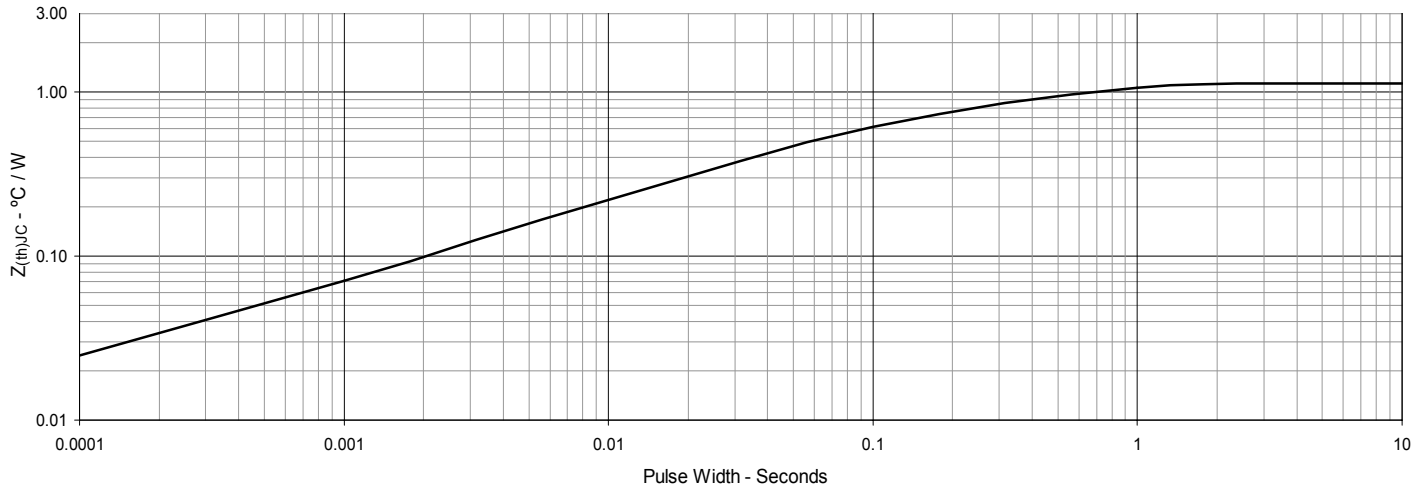
**Fig. 9. Gate Charge**



**Fig. 10. Capacitance**



**Fig. 11. Maximum Transient Thermal Impedance**





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