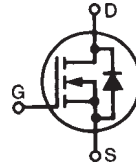


High Voltage MOSFET

IXTA 1N100
IXTP 1N100

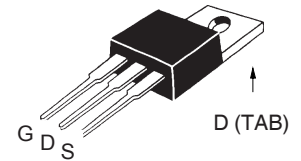
$V_{DSS} = 1000\text{ V}$
 $I_{D25} = 1.5\text{ A}$
 $R_{DS(on)} = 11\ \Omega$

N-Channel Enhancement Mode
Avalanche Energy Rated

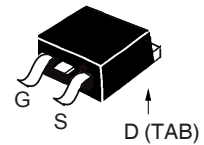


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	1000	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1\text{ M}\Omega$	1000	V
V_{GS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}$	1.5	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	6	A
I_{AR}		1.5	A
E_{AR}	$T_C = 25^\circ\text{C}$	6	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	200	mJ
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 18\ \Omega$	3	V/ns
P_D	$T_C = 25^\circ\text{C}$	54	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		4	g
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	$^\circ\text{C}$

TO-220AB (IXTP)



TO-263 AA (IXTA)



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard packages
- High voltage, Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Fast switching times

Applications

- Switch-mode and resonant-mode power supplies
- Flyback inverters
- DC choppers
- High frequency matching

Advantages

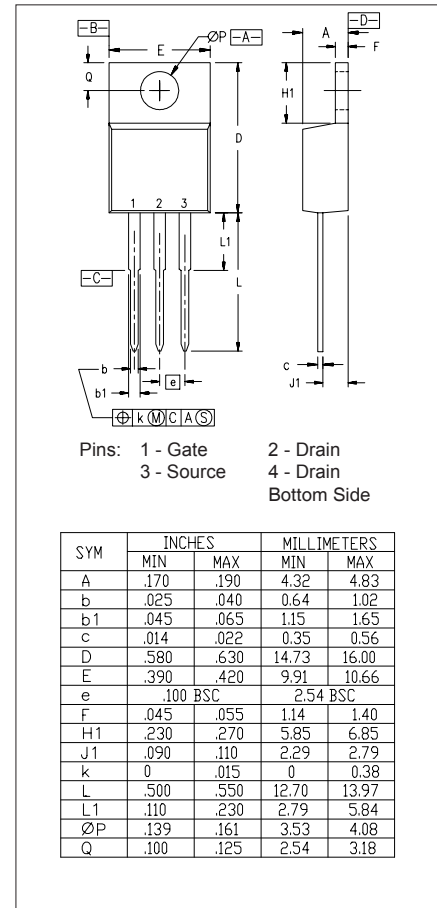
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$	1000		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 25\ \mu\text{A}$	2.5		4.5 V
I_{GSS}	$V_{GS} = \pm 30\text{ V}_{DC}$, $V_{DS} = 0$			$\pm 100\text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0\text{ V}$			25 μA 500 μA $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 1.0\text{ A}$ Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			11 Ω

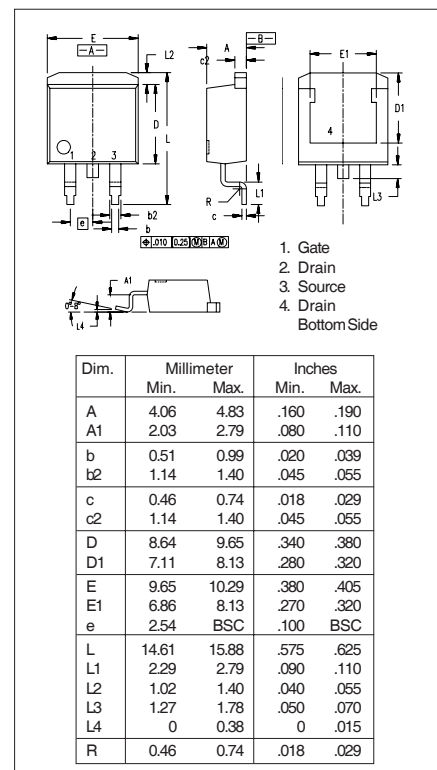
Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	$V_{DS} = 20\text{ V}; I_D = 1.0\text{ A}$, pulse test	0.8	1.5	S
C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		400	pF
C_{oss}			37	pF
C_{rss}			13	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 1\text{ A}$ $R_G = 18\Omega$, (External)		18	ns
t_r			19	ns
$t_{d(off)}$			20	ns
t_f			18	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 1\text{ A}$		14.5	nC
Q_{gs}			3.0	nC
Q_{gd}			7.5	nC
R_{thJC}			2.3	K/W
R_{thCK}	(IXTP)	0.50		K/W

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
I_S	$V_{GS} = 0\text{ V}$			1.5 A
I_{SM}	Repetitive; pulse width limited by T_{JM}			6 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			1.8 V
t_{rr}	$I_F = I_S, -di/dt = 100\text{ A}/\mu\text{s}, V_R = 100\text{ V}$		710	ns

TO-220 AD Dimensions



TO-263 AA Outline



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	

Fig. 1. Output Characteristics @ 25°C

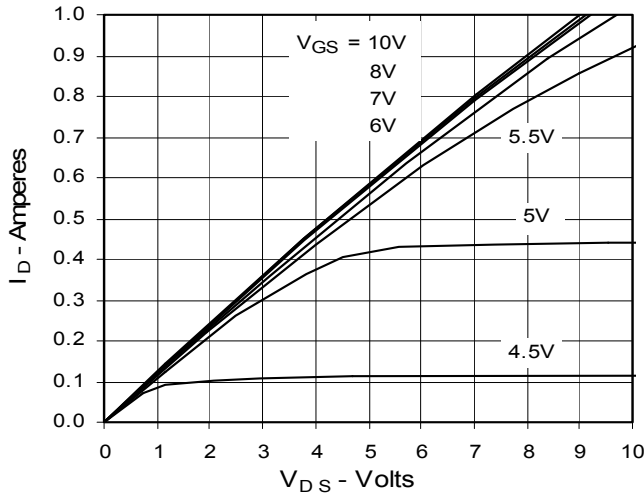


Fig. 2. Extended Output Characteristics @ 25°C

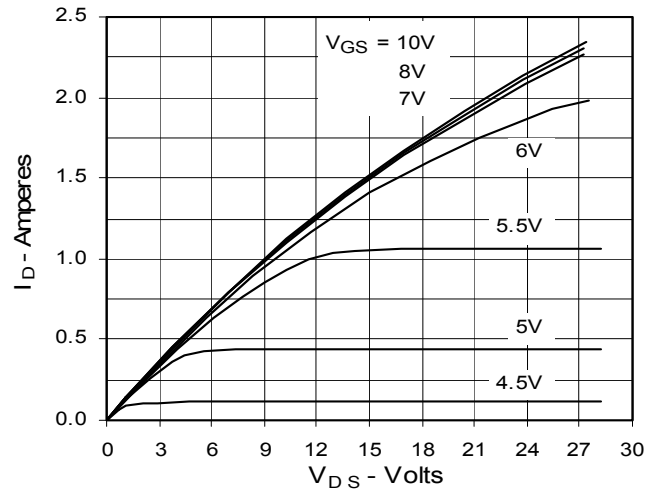


Fig. 3. Output Characteristics @ 125°C

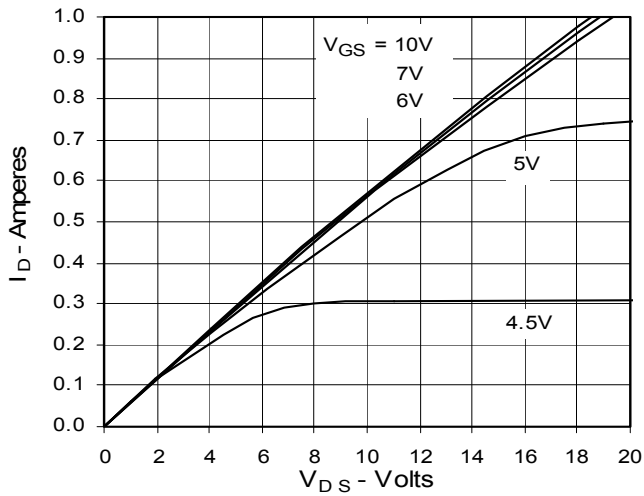


Fig. 4. Normalized $R_{DS(on)}$ vs. Junction Temperature

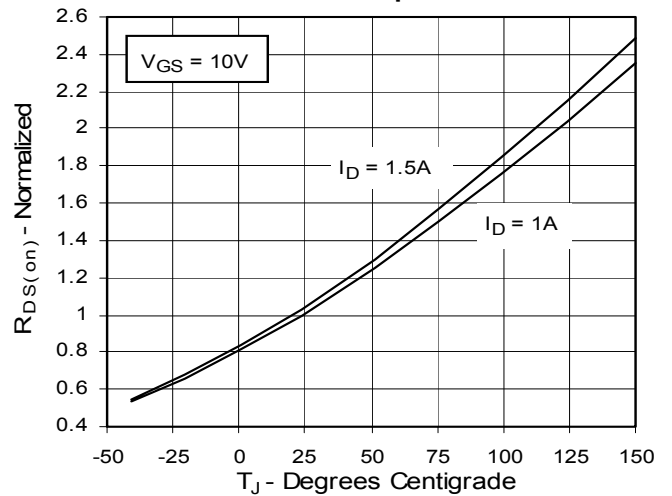


Fig. 5. Normalized $R_{DS(on)}$ vs. I_D

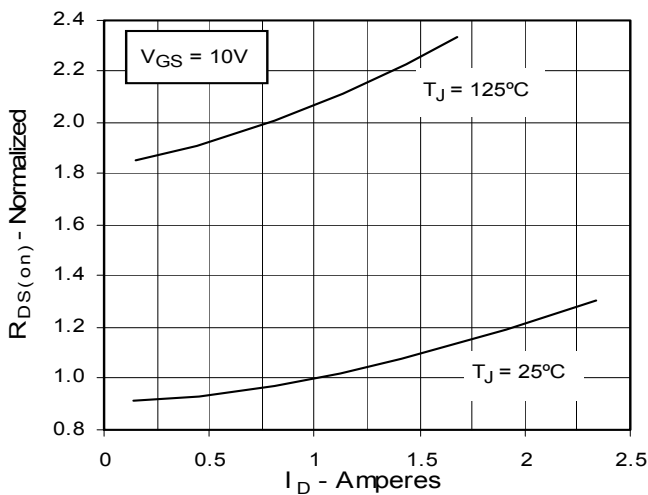


Fig. 6. Drain Current vs. Case Temperature

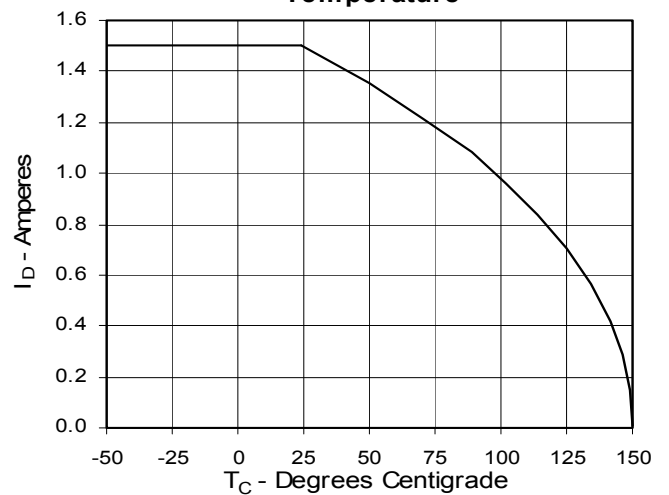


Fig. 7. Input Admittance

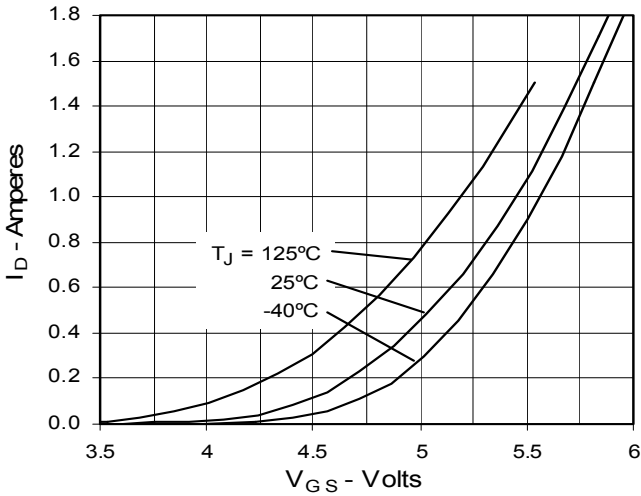


Fig. 8. Transconductance

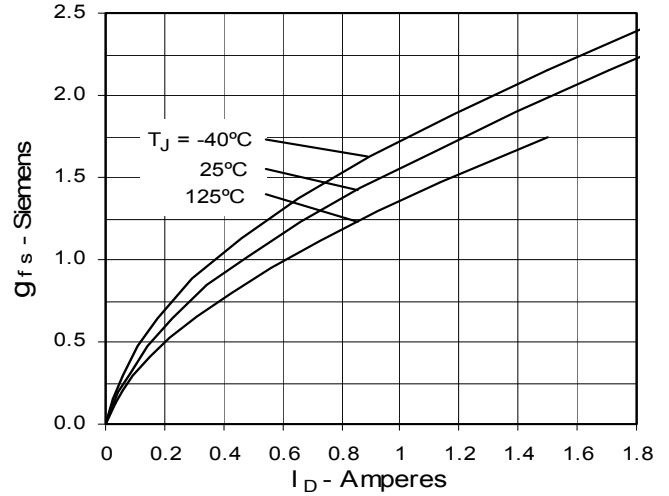


Fig. 9. Source Current vs. Source-To-Drain Voltage

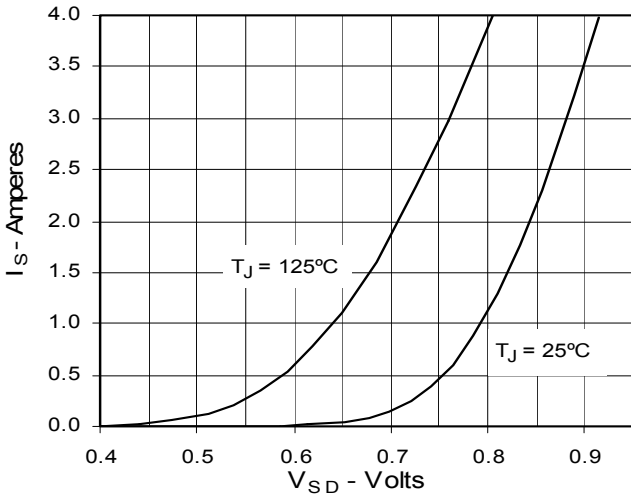


Fig. 10. Gate Charge

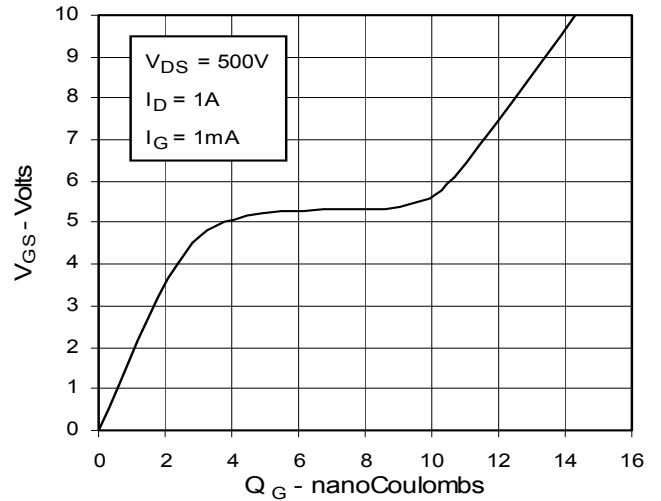


Fig. 11. Capacitance

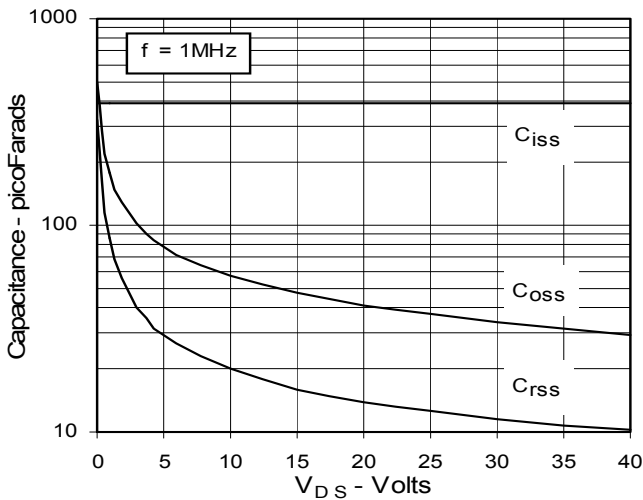
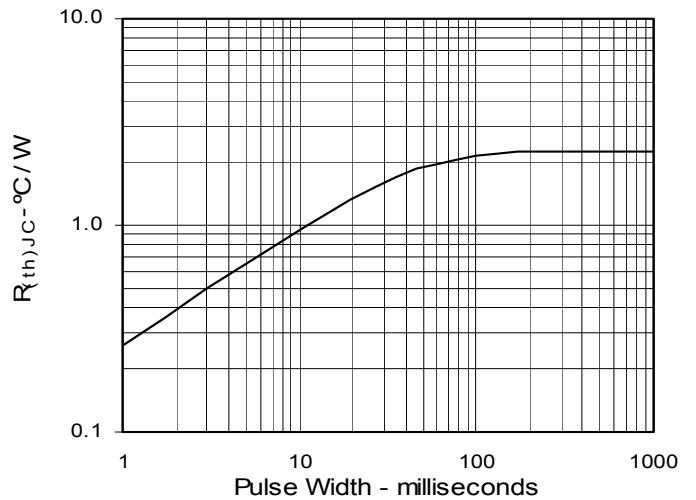


Fig. 13. Maximum Transient Thermal Resistance





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