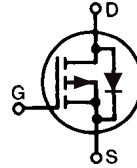


# Standard Power MOSFET

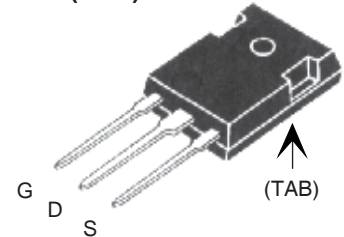
## IXTH50P10 IXTT50P10

$V_{DSS} = -100V$   
 $I_{D25} = -50A$   
 $R_{DS(on)} \leq 55m\Omega$

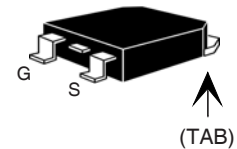
P-Channel Enhancement Mode  
Avalanche Rated



TO-247 (IXTH)



TO-268 (IXTT)



G = Gate                      D = Drain  
 S = Source                    TAB = Drain

Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ C$ to $150^\circ C$	-100	V
$V_{DGR}$	$T_J = 25^\circ C$ to $150^\circ C$ , $R_{GS} = 1M\Omega$	-100	V
$V_{GSS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ C$	- 50	A
$I_{DM}$	$T_C = 25^\circ C$ , pulse width limited by $T_{JM}$	- 200	A
$I_A$	$T_C = 25^\circ C$	- 50	A
$E_{AS}$	$T_C = 25^\circ C$	30	mJ
$P_D$	$T_C = 25^\circ C$	300	W
$T_J$		- 55 ... +150	$^\circ C$
$T_{JM}$		150	$^\circ C$
$T_{stg}$		- 55 ... +150	$^\circ C$
$T_L$	1.6mm (0.062 in.) from case for 10s	300	$^\circ C$
$T_{SOLD}$	Plastic body for 10s	260	$^\circ C$
$M_d$	Mounting torque (TO-247)	1.13 / 10	Nm/lb.in.
Weight	TO-247	6	g
	TO-268	5	g

### Features

- International standard packages  
JEDEC TO-247 AD
- Low  $R_{DS(ON)}$  HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance (< 5nH)  
- easy to drive and to protect

### Applications

- High side switching
- Push-pull amplifiers
- DC Choppers
- Automatic test equipment

### Advantages

- Easy to mount with 1 screw  
(isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions ( $T_J = 25^\circ C$ , unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0V$ , $I_D = -250 \mu A$	-100		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250 \mu A$	- 3.0		- 5.0 V
$I_{GSS}$	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			$\pm 100$ nA
$I_{DSS}$	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0V$			- 25 $\mu A$ -1 mA
$R_{DS(on)}$	$V_{GS} = -10V$ , $I_D = 0.5 \cdot I_{D25}$ , Note 1			55 m $\Omega$

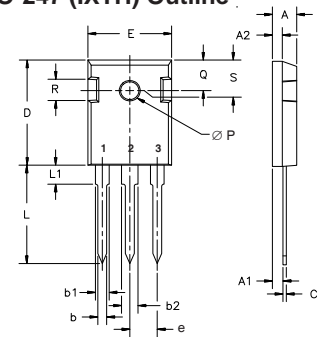
Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = -10\text{V}$ , $I_D = 0.5 \cdot I_{D25}$ , Note 1	13	22	S
$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = -25\text{V}$ , $f = 1\text{MHz}$		4350	pF
$C_{oss}$			1505	pF
$C_{rss}$			733	pF
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = -10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 0.5 \cdot I_{D25}$ $R_G = 4.7\Omega$ (External)		46	ns
$t_r$			39	ns
$t_{d(off)}$			86	ns
$t_f$			38	ns
$Q_{g(on)}$	$V_{GS} = -10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 0.5 \cdot I_{D25}$		140	nC
$Q_{gs}$			25	nC
$Q_{gd}$			85	nC
$R_{thJC}$			0.42	$^\circ\text{C/W}$
$R_{thCS}$		0.25		$^\circ\text{C/W}$

### Source-Drain Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
$I_s$	$V_{GS} = 0\text{V}$			- 50 A
$I_{SM}$	Repetitive, pulse width limited by $T_{JM}$			- 200 A
$V_{SD}$	$I_F = -25\text{A}$ , $V_{GS} = 0\text{V}$ , Note 1			- 3.0 V
$t_{rr}$	$I_F = -25\text{A}$ , $di/dt = -100\text{A}/\mu\text{s}$ , $V_R = -50\text{V}$ , $V_{GS} = 0\text{V}$	180		ns

Note 1: Pulse test,  $t \leq 300\mu\text{s}$ ; duty cycle,  $d \leq 2\%$ .

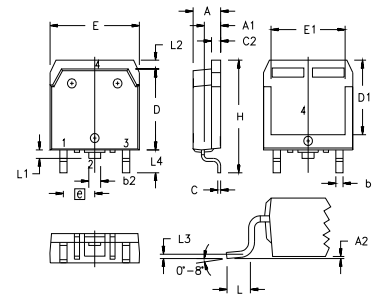
### TO-247 (IXTH) Outline



Terminals: 1 - Gate 2 - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A <sub>1</sub>	2.2	2.54	.087	.102
A <sub>2</sub>	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b <sub>1</sub>	1.65	2.13	.065	.084
b <sub>2</sub>	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216

### TO-268 (IXTT) Outline

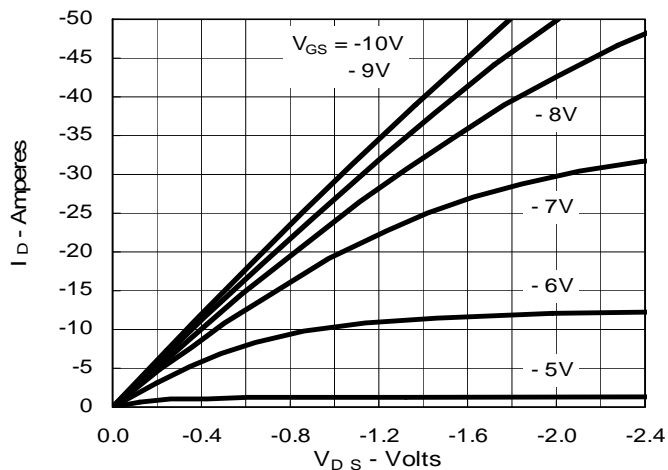


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

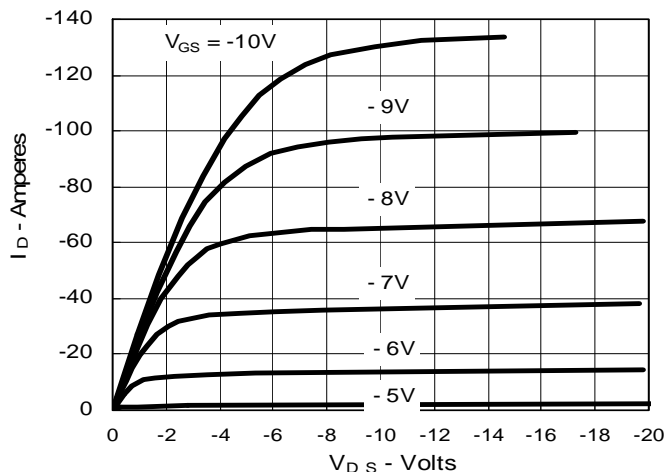
IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2  
by one or more of the following U.S. patents: 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2  
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

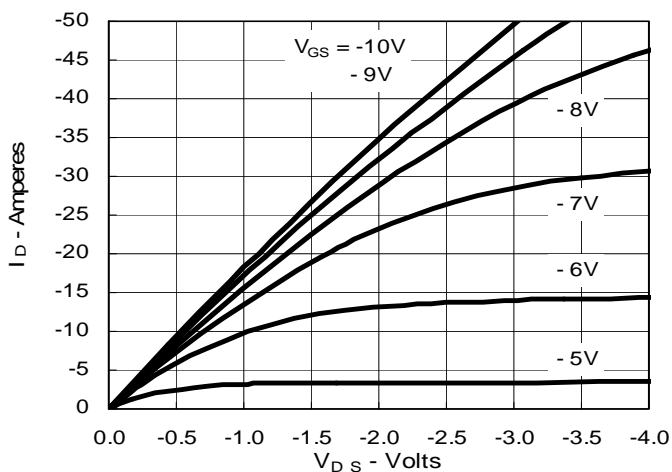
**Fig. 1. Output Characteristics @ 25°C**



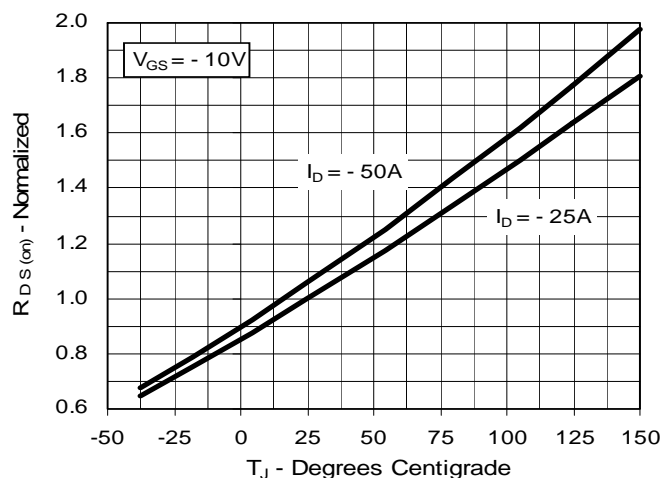
**Fig. 2. Extended Output Characteristics @ 25°C**



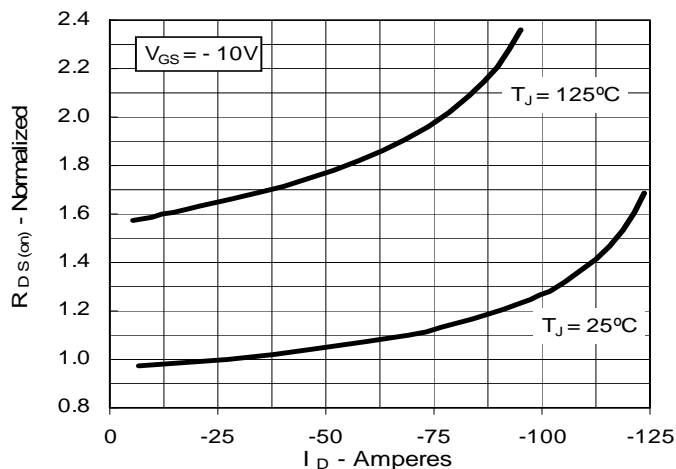
**Fig. 3. Output Characteristics @ 125°C**



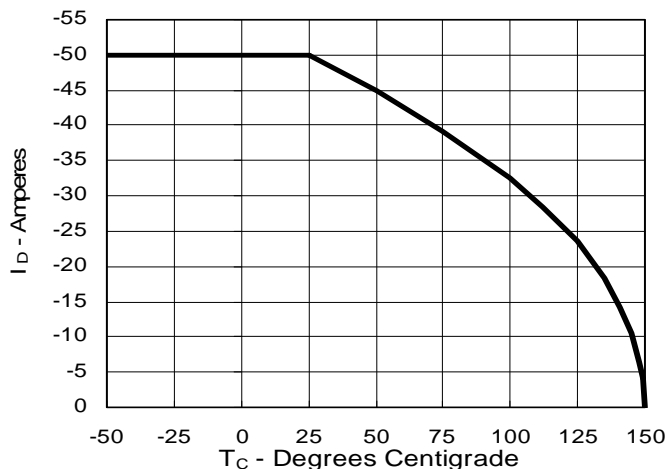
**Fig. 4.  $R_{DS(on)}$  Normalized to 0.5  $I_{D25}$  Value vs. Junction Temperature**



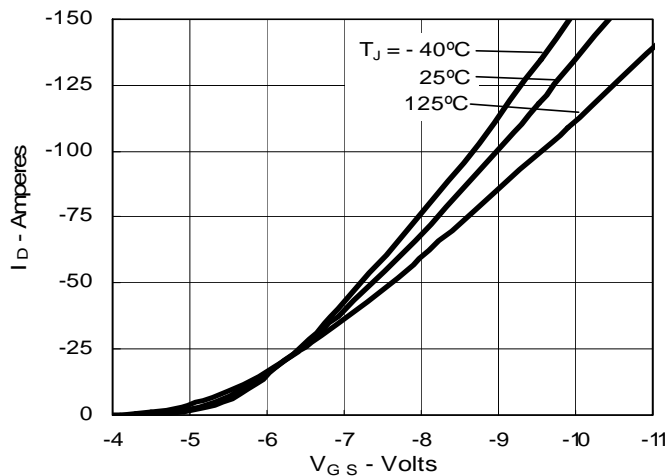
**Fig. 5.  $R_{DS(on)}$  Normalized to 0.5  $I_{D25}$  Value vs.  $I_D$**



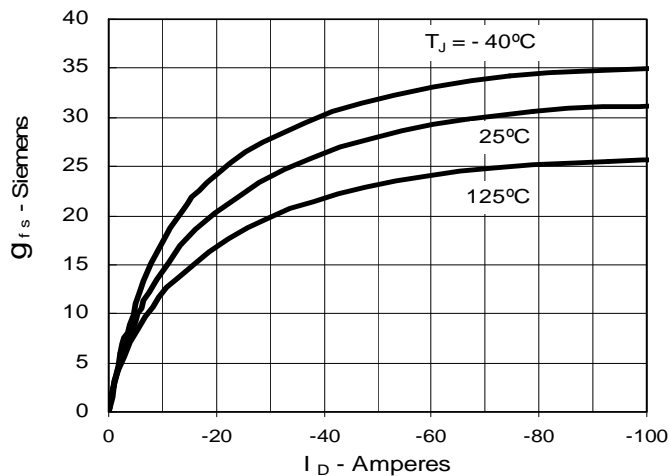
**Fig. 6. Drain Current vs. Case Temperature**



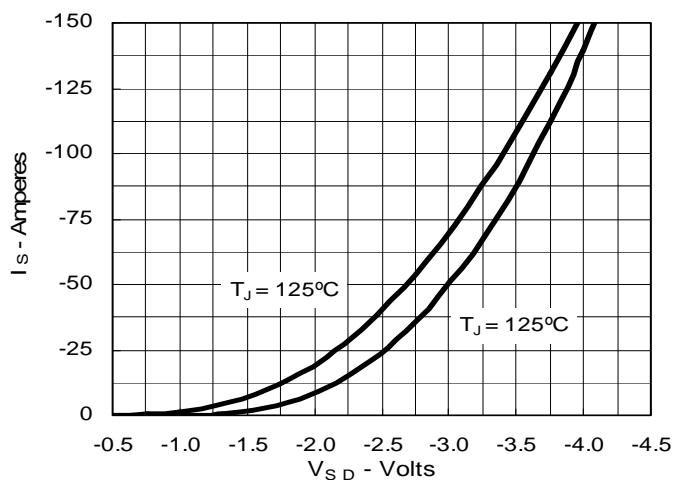
**Fig. 7. Input Admittance**



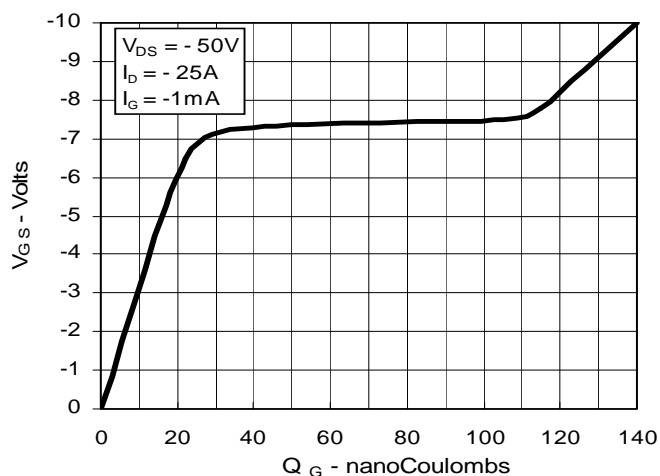
**Fig. 8. Transconductance**



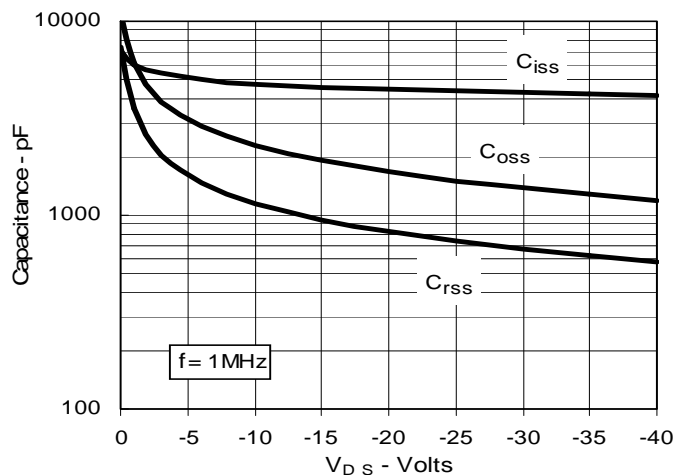
**Fig. 9. Source Current vs. Source-To-Drain Voltage**



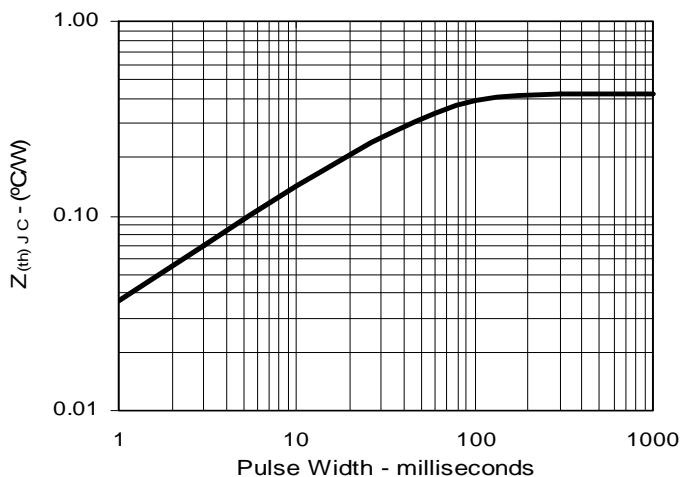
**Fig. 10. Gate Charge**



**Fig. 11. Capacitance**



**Fig. 12. Maximum Transient Thermal Impedance**





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