



High Efficiency Thyristor

$$V_{RRM} = 2 \times 1200 \text{ V}$$

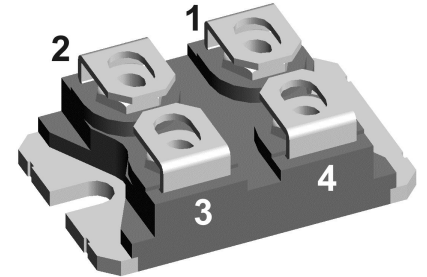
$$I_{TAV} = 60 \text{ A}$$

$$V_T = 1.09 \text{ V}$$

Phase leg

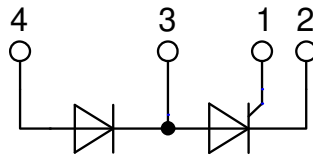
Part number

CLA60PD1200NA



Backside: Isolated

E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: SOT-227B (minibloc)

- Isolation Voltage: 3000 V~
- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0
- Base plate: Copper internally DCB isolated
- Advanced power cycling

Disclaimer Notice

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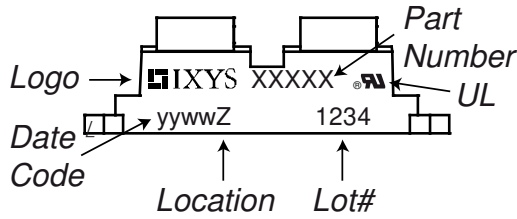


Rectifier			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1200	V
I_{RD}	reverse current, drain current	$V_{R/D} = 1200 V$	$T_{VJ} = 25^{\circ}C$		50	μA
		$V_{R/D} = 1200 V$	$T_{VJ} = 125^{\circ}C$		5	mA
V_T	forward voltage drop	$I_T = 60 A$	$T_{VJ} = 25^{\circ}C$		1.16	V
		$I_T = 120 A$			1.39	V
		$I_T = 60 A$	$T_{VJ} = 125^{\circ}C$		1.09	V
		$I_T = 120 A$			1.38	V
I_{TAV}	average forward current	$T_C = 100^{\circ}C$	$T_{VJ} = 150^{\circ}C$		60	A
$I_{T(RMS)}$	RMS forward current	180° sine			94	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0.79	V
r_T	slope resistance				4.8	m Ω
R_{thJC}	thermal resistance junction to case				0.55	K/W
R_{thCH}	thermal resistance case to heatsink			0.1		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		220	W
I_{TSM}	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		1.10	kA
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		1.19	kA
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		935	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		1.01	kA
I^2t	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		6.05	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		5.89	kA ² s
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		4.37	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		4.25	kA ² s
C_J	junction capacitance	$V_R = 400 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		43	pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W
		$t_p = 300 \mu s$			1	W
P_{GAV}	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C; f = 50 \text{ Hz}$	repetitive, $I_T = 180 A$		150	A/ μs
		$t_p = 200 \mu s; di_G/dt = 0.45 A/\mu s;$ $I_G = 0.45 A; V = \frac{2}{3} V_{DRM}$	non-repet., $I_T = 60 A$		500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty; \text{ method 1 (linear voltage rise)}$	$T_{VJ} = 150^{\circ}C$		1000	V/ μs
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1.5	V
			$T_{VJ} = -40^{\circ}C$		1.6	V
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		40	mA
			$T_{VJ} = -40^{\circ}C$		80	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0.2	V
I_{GD}	gate non-trigger current				5	mA
I_L	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		150	mA
		$I_G = 0.45 A; di_G/dt = 0.45 A/\mu s$				
I_H	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		100	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$ $I_G = 0.5 A; di_G/dt = 0.5 A/\mu s$	$T_{VJ} = 25^{\circ}C$		2	μs
t_q	turn-off time	$V_R = 100 V; I_T = 60 A; V = \frac{2}{3} V_{DRM}$ $di/dt = 10 A/\mu s \quad dv/dt = 20 V/\mu s \quad t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		150	μs



Package SOT-227B (minibloc)				Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit	
I_{RMS}	RMS current	per terminal			150	A	
T_{VJ}	virtual junction temperature		-40		150	°C	
T_{op}	operation temperature		-40		125	°C	
T_{stg}	storage temperature		-40		150	°C	
Weight					30	g	
M_D	mounting torque		1.1		1.5	Nm	
M_T	terminal torque		1.1		1.5	Nm	
$d_{Spp/App}$	creepage distance on surface striking distance through air	terminal to terminal	10.5	3.2		mm	
$d_{Spb/Apb}$		terminal to backside	8.6	6.8		mm	
V_{ISOL}	isolation voltage	t = 1 second	3000			V	
		t = 1 minute	2500			V	

Product Marking



Part description

- C = Thyristor (SCR)
- L = High Efficiency Thyristor
- A = (up to 1200V)
- 60 = Current Rating [A]
- PD = Phase leg
- 1200 = Reverse Voltage [V]
- NA = SOT-227B (minibloc)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA60PD1200NA	CLA60PD1200NA	Tube	10	513121

Similar Part	Package	Voltage class
CLA100PD1200NA	SOT-227B (minibloc)	1200

Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 150^{\circ}C$

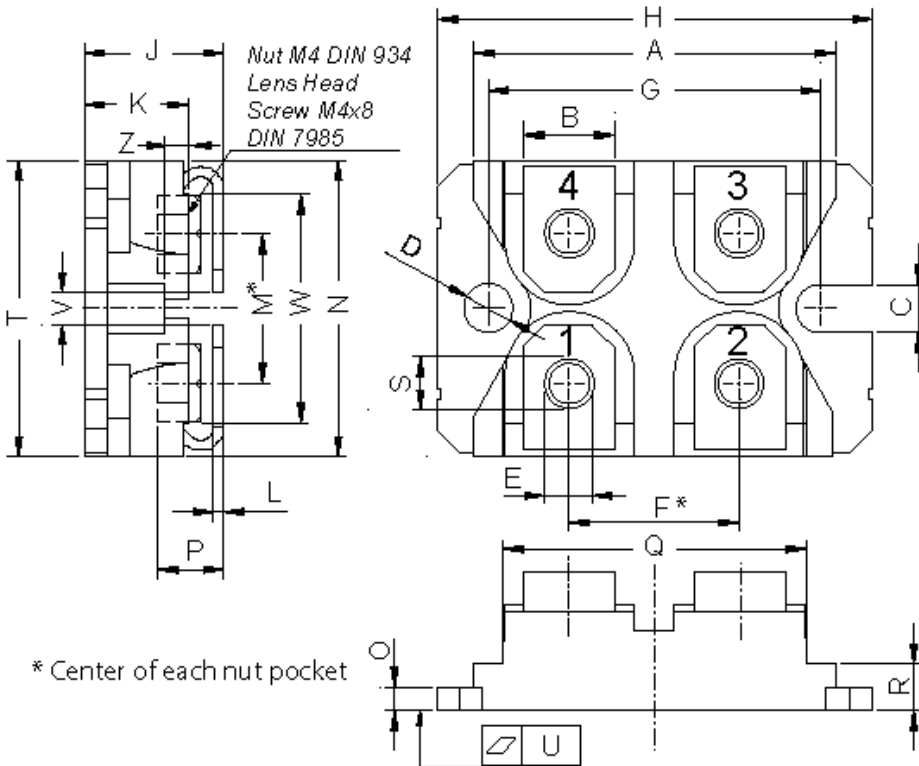


Thyristor

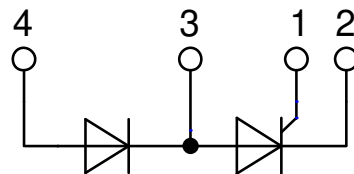
$V_{0\ max}$	threshold voltage	0.79	V
$R_{0\ max}$	slope resistance *	3	mΩ



Outlines SOT-227B (minibloc)



Dim.	Millimeter		Inches	
	min	max	min	max
A	31.50	31.88	1.240	1.255
B	7.80	8.20	0.307	0.323
C	4.09	4.29	0.161	0.169
D	4.09	4.29	0.161	0.169
E	4.09	4.29	0.161	0.169
F	14.91	15.11	0.587	0.595
G	30.12	30.30	1.186	1.193
H	37.80	38.23	1.488	1.505
J	11.68	12.22	0.460	0.481
K	8.92	9.60	0.351	0.378
L	0.74	0.84	0.029	0.033
M	12.50	13.10	0.492	0.516
N	25.15	25.42	0.990	1.001
O	1.95	2.13	0.077	0.084
P	4.95	6.20	0.195	0.244
Q	26.54	26.90	1.045	1.059
R	3.94	4.42	0.155	0.167
S	4.55	4.85	0.179	0.191
T	24.59	25.25	0.968	0.994
U	-0.05	0.10	-0.002	0.004
V	3.20	5.50	0.126	0.217
W	19.81	21.08	0.780	0.830
Z	2.50	2.70	0.098	0.106



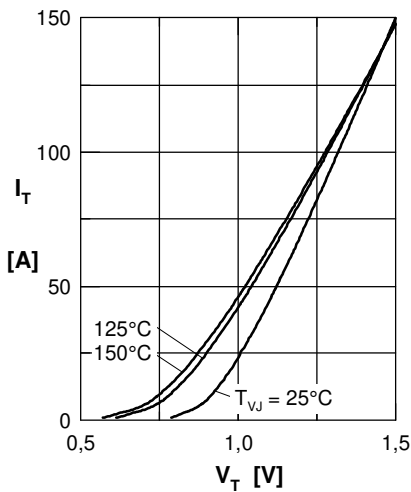
Thyristor


Fig. 1 Forward characteristics

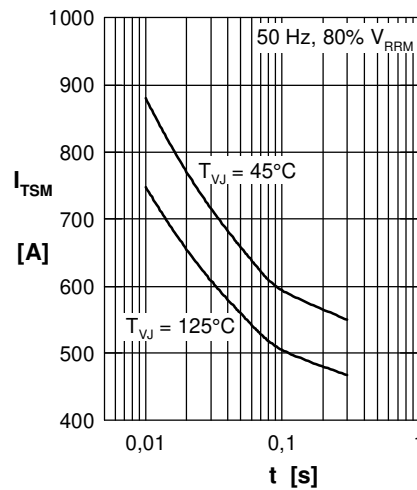


Fig. 2 Surge overload current

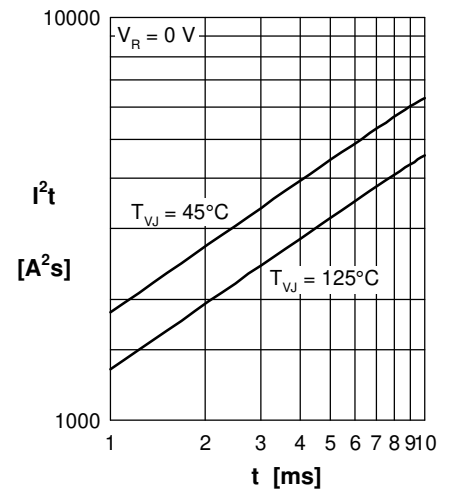
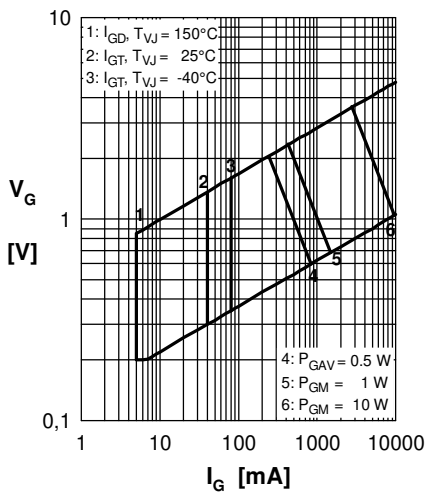

 Fig. 3 I^2t versus time (1-10 ms)


Fig. 4 Gate trigger characteristics

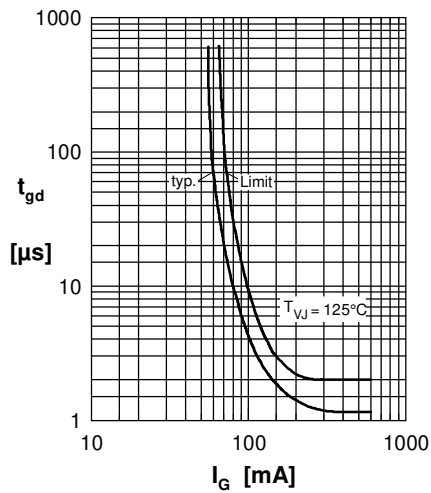


Fig. 5 Gate controlled delay time

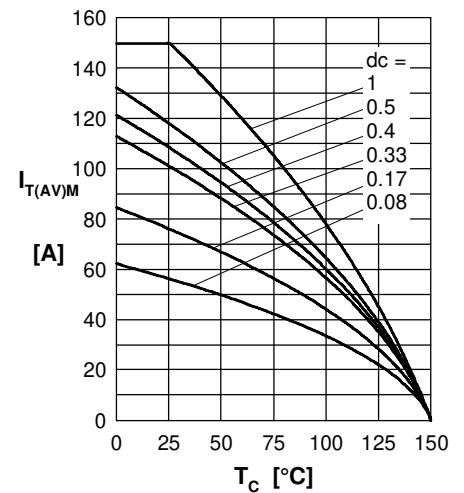


Fig. 6 Max. forward current at case temperature

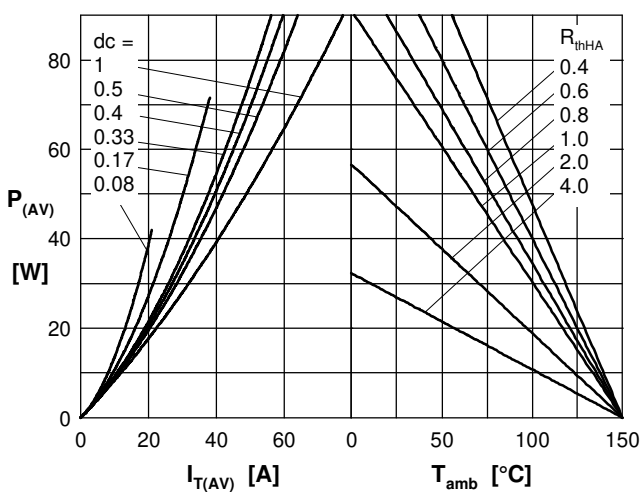
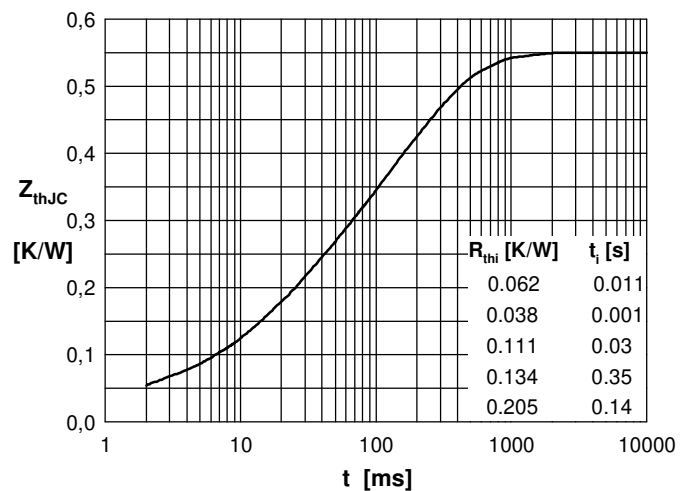

 Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance junction to case