



# High Efficiency Thyristor

$V_{RRM} = 1200\text{ V}$

$I_{TAV} = 20\text{ A}$

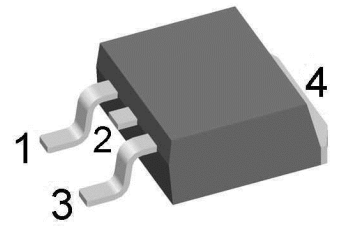
$V_T = 1.54\text{ V}$

SemiFast  
Single Thyristor

Part number

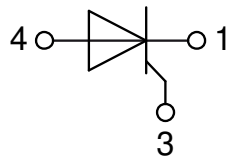
**CLE20E1200PC**

Marking on Product: CLE20E1200PC



Backside: anode

ESD Level: H3B



**Features / Advantages:**

- Thyristor for line and moderate frequencies
- Short turn-off time
- Planar passivated chip
- Long-term stability

**Applications:**

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

**Package:** TO-263 (D2Pak)

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

**Disclaimer Notice**

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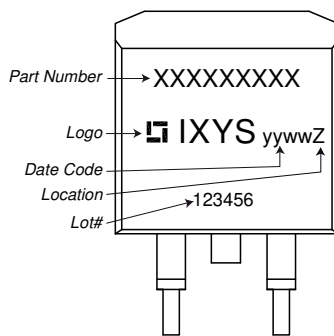


Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1200	V
$I_{RD}$	reverse current, drain current	$V_{R/D} = 1200 V$	$T_{VJ} = 25^{\circ}C$		100	$\mu A$
		$V_{R/D} = 1200 V$	$T_{VJ} = 125^{\circ}C$		2	mA
$V_T$	forward voltage drop	$I_T = 20 A$	$T_{VJ} = 25^{\circ}C$		1.54	V
		$I_T = 40 A$			2.03	V
		$I_T = 20 A$	$T_{VJ} = 125^{\circ}C$		1.54	V
		$I_T = 40 A$			2.17	V
$I_{TAV}$	average forward current	$T_C = 95^{\circ}C$ 180° sine	$T_{VJ} = 150^{\circ}C$		20	A
$V_{T0}$	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0.87	V
$r_T$	slope resistance				34	m $\Omega$
$R_{thJC}$	thermal resistance junction to case				1	K/W
$R_{thCH}$	thermal resistance case to heatsink			0.25		K/W
$P_{tot}$	total power dissipation		$T_C = 25^{\circ}C$		125	W
$I_{TSM}$	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		160	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		175	A
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		135	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		145	A
$I^2t$	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		130	A <sup>2</sup> s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		125	A <sup>2</sup> s
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		91	A <sup>2</sup> s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		87	A <sup>2</sup> s
$C_J$	junction capacitance	$V_R = 400 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		7	pF
$P_{GM}$	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		5	W
		$t_p = 300 \mu s$			2.5	W
$P_{GAV}$	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^{\circ}C; f = 50 \text{ Hz}$ repetitive, $I_T = 60 A$			100	A/ $\mu s$
		$t_p = 200 \mu s; di_G/dt = 0.15 A/\mu s;$ $I_G = 0.15 A; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 20 A$			500	A/ $\mu s$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty$ ; method 1 (linear voltage rise)	$T_{VJ} = 125^{\circ}C$		500	V/ $\mu s$
$V_{GT}$	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1.5	V
			$T_{VJ} = -40^{\circ}C$		2.5	V
$I_{GT}$	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		40	mA
			$T_{VJ} = -40^{\circ}C$		70	mA
$V_{GD}$	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}C$		0.2	V
$I_{GD}$	gate non-trigger current				3	mA
$I_L$	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		60	mA
		$I_G = 0.1 A; di_G/dt = 0.1 A/\mu s$				
$I_H$	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		50	mA
$t_{gd}$	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$ $I_G = 0.1 A; di_G/dt = 0.1 A/\mu s$	$T_{VJ} = 25^{\circ}C$		2	$\mu s$
$t_q$	turn-off time	$V_R = 20 V; I_T = 20 A; V = \frac{2}{3} V_{DRM}$ $di/dt = 10 A/\mu s \quad dv/dt = 1000 V/\mu s \quad t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$	100		$\mu s$



Package TO-263 (D2Pak)			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$I_{RMS}$	RMS current	per terminal			35	A
$T_{VJ}$	virtual junction temperature		-40		150	°C
$T_{op}$	operation temperature		-40		125	°C
$T_{stg}$	storage temperature		-40		150	°C
<b>Weight</b>				1.5		g
$F_C$	mounting force with clip		20		60	N

**Product Marking**



**Part description**

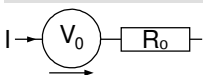
- C = Thyristor (SCR)
- L = High Efficiency Thyristor
- E = Semifast (up to 1200V)
- 20 = Current Rating [A]
- E = Single Thyristor
- 1200 = Reverse Voltage [V]
- PC = TO-263AB (D2Pak) (2)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLE20E1200PC-TRL	CLE20E1200PC	Tape & Reel	800	512774
Alternative	CLE20E1200PC-TUB	CLE20E1200PC	Tube	50	523602

**Equivalent Circuits for Simulation**

*\* on die level*

$T_{VJ} = 150^{\circ}C$

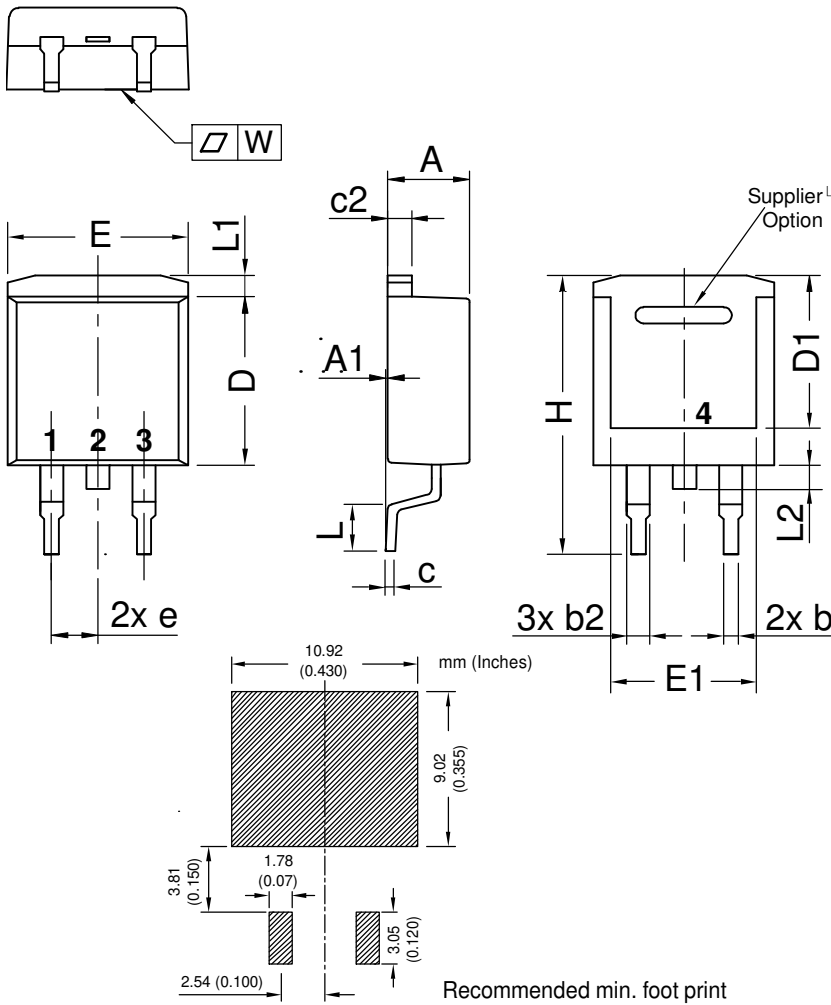


**Thyristor**

$V_{0\ max}$	threshold voltage	0.87	V
$R_{0\ max}$	slope resistance *	36	mΩ

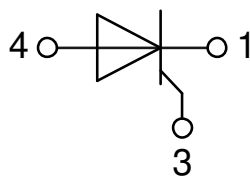


**Outlines TO-263 (D2Pak)**



Dim.	Millimeter		Inches	
	min	max	min	max
A	4.06	4.83	0.160	0.190
A1	typ. 0.10		typ. 0.004	
A2	2.41		0.095	
b	0.51	0.99	0.020	0.039
b2	1.14	1.40	0.045	0.055
c	0.40	0.74	0.016	0.029
c2	1.14	1.40	0.045	0.055
D	8.38	9.40	0.330	0.370
D1	8.00	8.89	0.315	0.350
D2	2.5		0.098	
E	9.65	10.41	0.380	0.410
E1	6.22	8.50	0.245	0.335
e	2,54 BSC		0,100 BSC	
e1	4.28		0.169	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	1.02	1.68	0.040	0.066
W	typ. 0.02	0.040	typ. 0.0008	0.002

*All dimensions conform with and/or within JEDEC standard.*



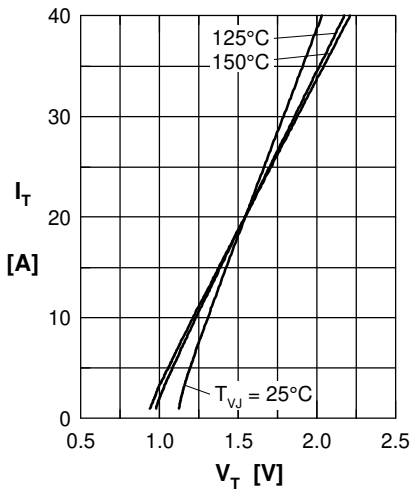
**Thyristor**


Fig. 1 Forward characteristics

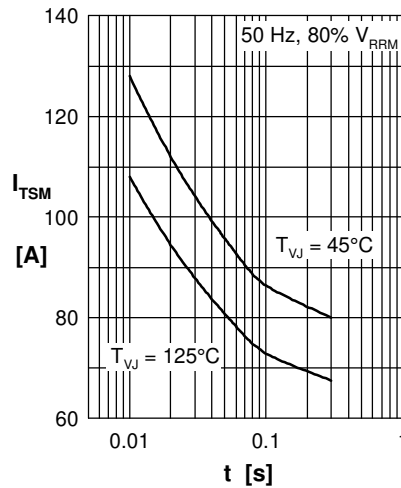


Fig. 2 Surge overload current

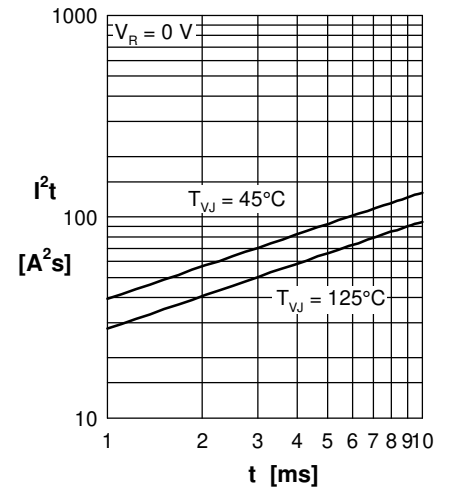
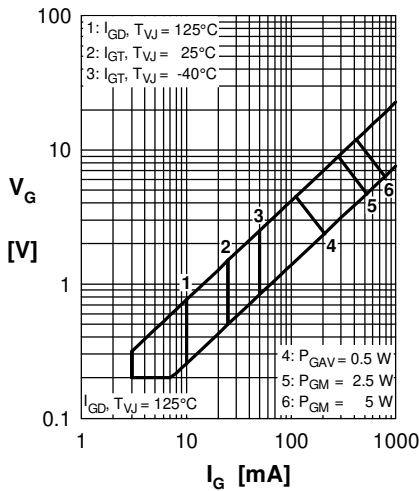

 Fig. 3  $I^2t$  versus time (1-10 ms)


Fig. 4 Gate trigger characteristics

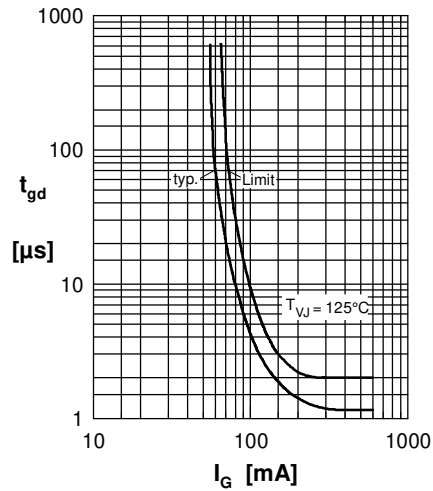


Fig. 5 Gate controlled delay time

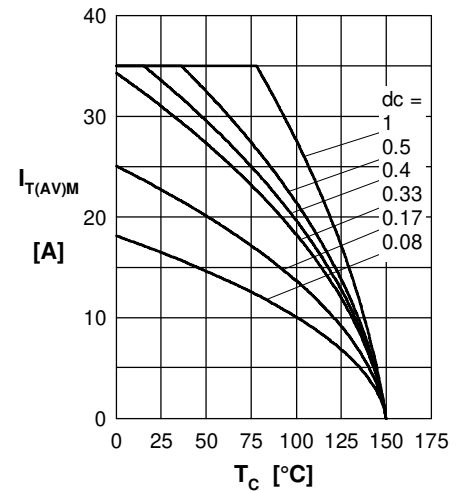


Fig. 6 Max. forward current at case temperature

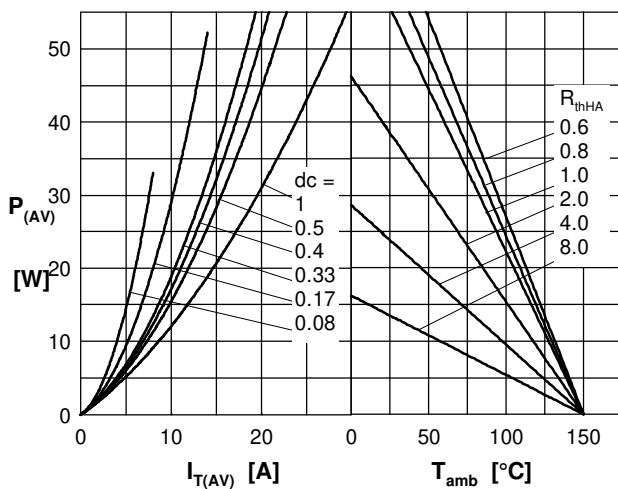
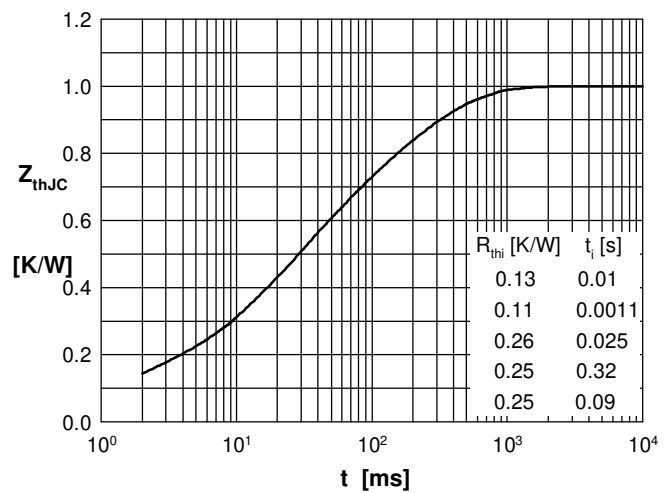

 Fig. 7a Power dissipation versus direct output current  
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance junction to case