

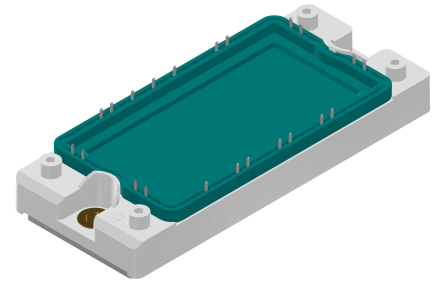
Thyristor Module

3~ Rectifier
$V_{RRM} = 1800\text{ V}$
$I_{DAV} = 120\text{ A}$
$I_{FSM} = 500\text{ A}$

3~ Rectifier Bridge, half-controlled (high-side) + free wheeling Diode

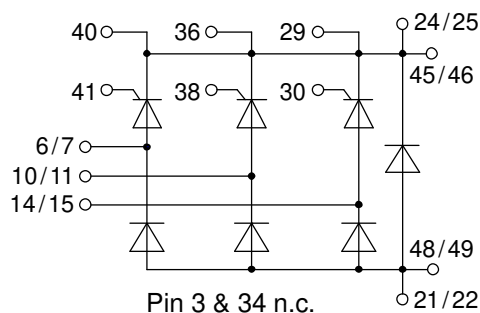
Part number

MCMA120UJ1800ED



Backside: isolated

 E72873



Features / Advantages:

- Thyristor/Standard Rectifier for line frequency
- Planar passivated chips
- Long-term stability
- Low forward voltage drop
- Leads suitable for PC board soldering
- Copper base plate with Direct Copper Bonded Al₂O₃-ceramic
- Improved temperature and power cycling

Applications:

- Diode for main rectification
- For single and three phase bridge configurations
- Supplies for DC power equipment
- Input rectifiers for PWM inverter
- Battery DC power supplies
- Field supply for DC motors

Package: E2-Pack

- Isolation Voltage: 3600 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Height: 17 mm
- Base plate: Copper internally DCB isolated
- Advanced power cycling
- Phase Change Material available

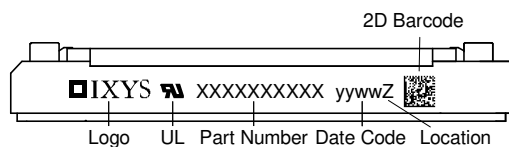
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Rectifier			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1900	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1800	V
I_{RD}	reverse current, drain current	$V_{R/D} = 1800 V$	$T_{VJ} = 25^{\circ}C$		50	μA
		$V_{R/D} = 1800 V$	$T_{VJ} = 125^{\circ}C$		10	mA
V_T	forward voltage drop	$I_T = 40 A$	$T_{VJ} = 25^{\circ}C$		1.33	V
		$I_T = 120 A$			1.70	V
		$I_T = 40 A$	$T_{VJ} = 125^{\circ}C$		1.36	V
		$I_T = 120 A$			1.88	V
I_{DAV}	bridge output current	$T_C = 80^{\circ}C$ rectangular $d = 1/3$	$T_{VJ} = 150^{\circ}C$		120	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}C$		0.83	V
r_T	slope resistance				13.6	m Ω
R_{thJC}	thermal resistance junction to case				0.65	K/W
R_{thCH}	thermal resistance case to heatsink			0.1		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		190	W
I_{TSM}	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		500	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		540	A
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		425	A
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		460	A
I^2t	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		1.25	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		1.22	kA ² s
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}C$		905	A ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		880	A ² s
C_J	junction capacitance	$V_R = 400 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		18	pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 150^{\circ}C$		10	W
		$t_p = 300 \mu s$			5	W
P_{GAV}	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C; f = 50 \text{ Hz}$ repetitive, $I_T = 120 A$			100	A/ μs
		$t_p = 200 \mu s; di_G/dt = 0.45 \text{ A}/\mu s;$ $I_G = 0.45 A; V = 2/3 V_{DRM}$ non-repet., $I_T = 40 A$			500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = 2/3 V_{DRM}$ $R_{GK} = \infty$; method 1 (linear voltage rise)	$T_{VJ} = 150^{\circ}C$		1000	V/ μs
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1.4	V
			$T_{VJ} = -40^{\circ}C$		1.6	V
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		70	mA
			$T_{VJ} = -40^{\circ}C$		150	mA
V_{GD}	gate non-trigger voltage	$V_D = 2/3 V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0.2	V
I_{GD}	gate non-trigger current				5	mA
I_L	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		150	mA
		$I_G = 0.45 A; di_G/dt = 0.45 \text{ A}/\mu s$				
I_H	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		100	mA
t_{gd}	gate controlled delay time	$V_D = 1/2 V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 0.45 A; di_G/dt = 0.45 \text{ A}/\mu s$				
t_q	turn-off time	$V_R = 100 V; I_T = 40 A; V = 2/3 V_{DRM}$ $di/dt = 10 \text{ A}/\mu s \quad dv/dt = 20 \text{ V}/\mu s \quad t_p = 200 \mu s$	$T_{VJ} = 125^{\circ}C$		500	μs



Package E2-Pack		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			50	A
T_{VJ}	virtual junction temperature		-40		150	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		125	°C
Weight				176		g
M_D	mounting torque		3		6	Nm
$d_{Spp/App}$	creepage distance on surface / striking distance through air	terminal to terminal	6.0			mm
$d_{Spb/Apb}$		terminal to backside	12.0			mm
V_{ISOL}	isolation voltage	t = 1 second t = 1 minute 50/60 Hz, RMS; $I_{ISOL} \leq 1$ mA	3600 3000			V V



Part description

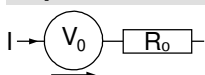
- M = Module
- C = Thyristor (SCR)
- M = Thyristor
- A = (up to 1800V)
- 120 = Current Rating [A]
- UJ = 3- Rectifier Bridge, half-controlled (high-side) + free wheeling Diode
- 1800 = Reverse Voltage [V]
- ED = E2-Pack

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCMA120UJ1800ED	MCMA120UJ1800ED	Box	6	510125

Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 150^{\circ}C$

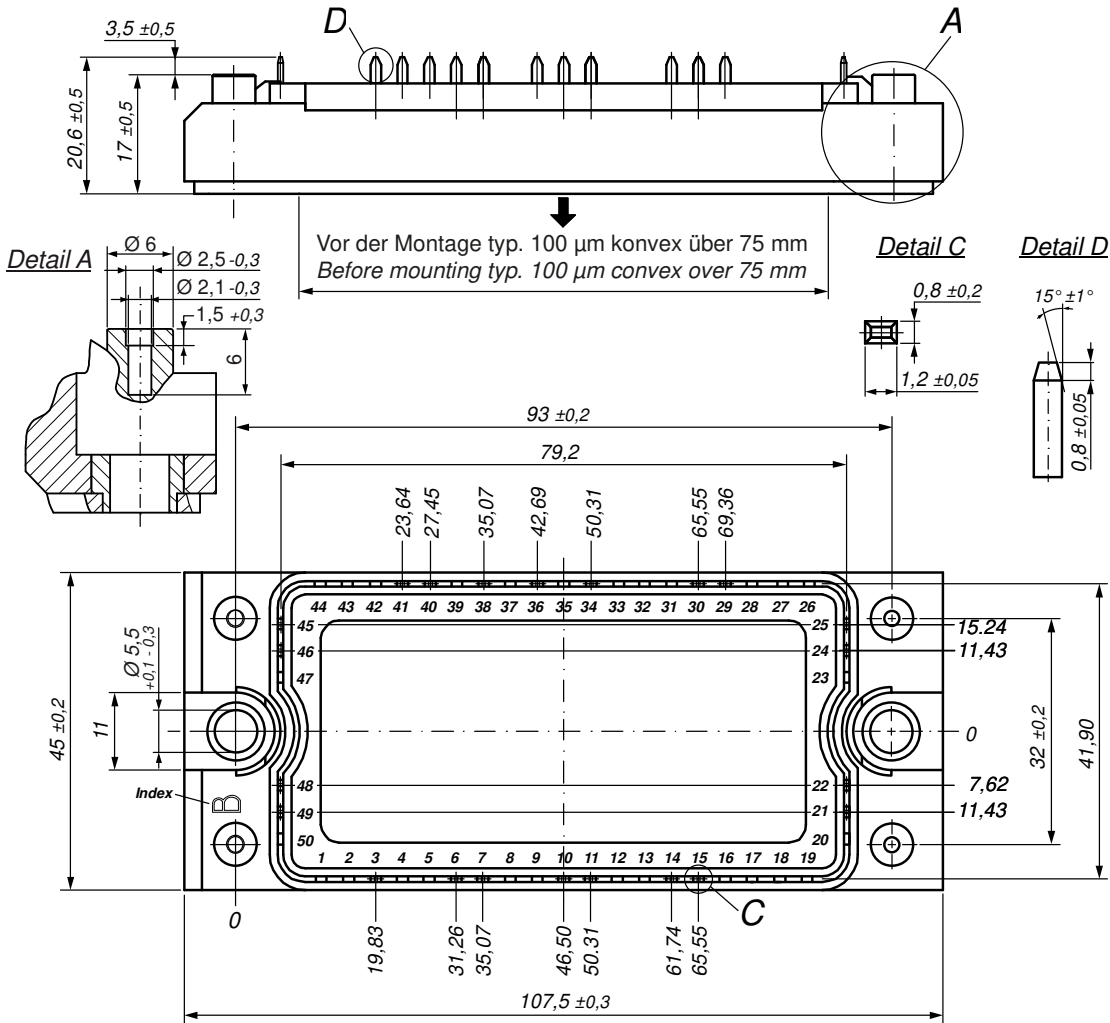


Thyristor

$V_{0\ max}$	threshold voltage	0.83	V
$R_{0\ max}$	slope resistance *	10.5	mΩ



Outlines E2-Pack

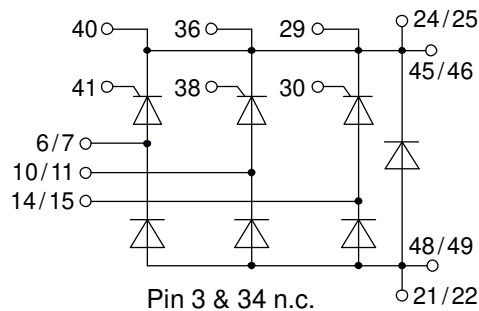


Bemerkung / Note:

- Nichttolerierete Maße nach / *Measure without tolerances according DIN ISO 2768-T1-m*
- PCB-Lochmuster / *PCB hole pattern: see pin position*
- Toleranz Pin-Position und PCB-Lochmuster / *Tolerance of pin position and PCB hole pattern: $\oplus 0.1$*
- Montageanleitung / *Mounting instruction: www.ixys.com Application note IXAN0024*

Detail A: PCB-Montage / *Mounting on PCB*

- Empfohlene, selbstschneidende Schraube / *Recommended, self-tapping screw: EJOT PT® (Größe / size: K25)*
- Max. Schraubenlänge / *Max. screw length: PCB-Dicke / thickness + 6 mm (max. Lochtiefe / hole depth)*
- Empfohlenes Drehmoment / *Recommended mounting torque: 1.5 Nm*



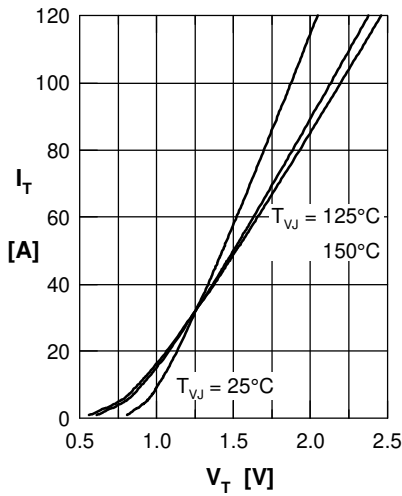
Thyristor


Fig. 1 Forward characteristics

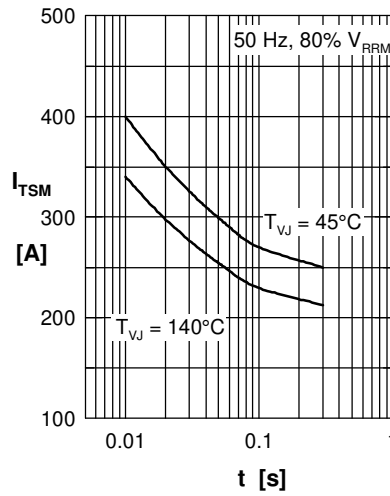
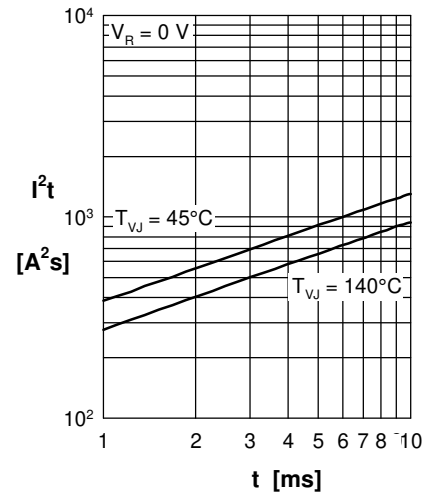
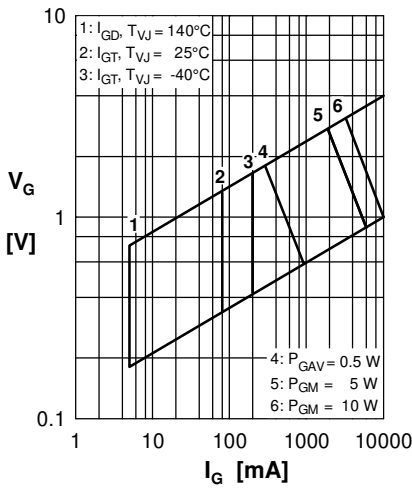

 Fig. 2 Surge overload current
 I_{TSM} : crest value, t : duration

 Fig. 3 I^2t versus time (1-10 s)


Fig. 4 Gate voltage & gate current

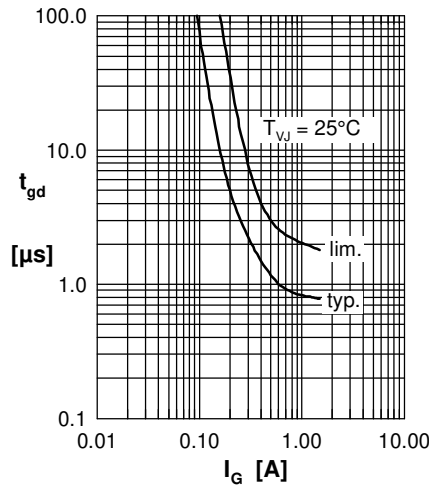
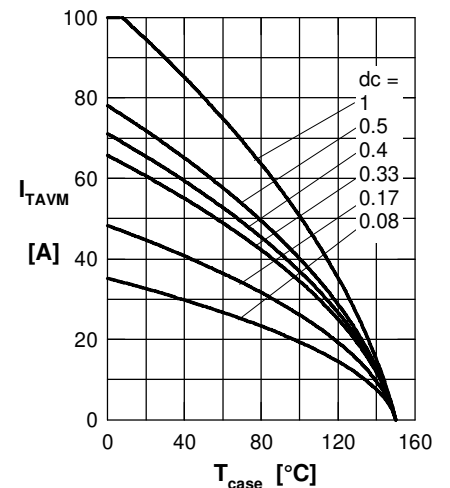

 Fig. 5 Gate controlled delay time t_{gd}


Fig. 6 Max. forward current at case temperature

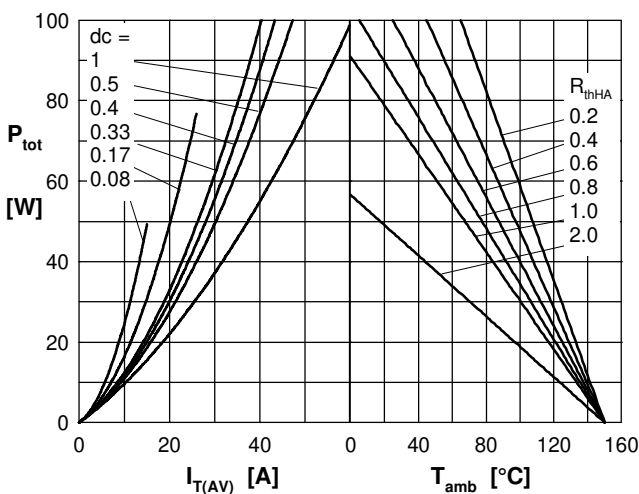
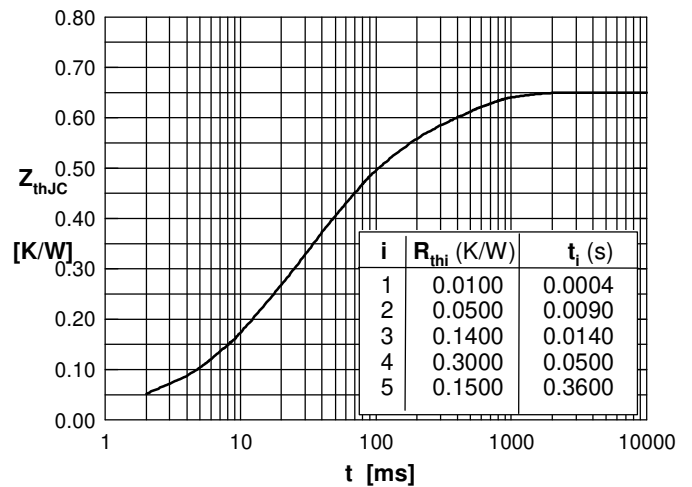

 Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance junction to case