

# High Voltage Thyristor \ Diode Module

$$V_{RRM} = 2 \times 2200 \text{ V}$$

$$I_{TAV} = 75 \text{ A}$$

$$V_T = 1.21 \text{ V}$$


Phase leg

Part number

**MCNA75PD2200TB**



Backside: isolated

 E72873



## Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al<sub>2</sub>O<sub>3</sub>-ceramic

## Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

## Package: TO-240AA

- Isolation Voltage: 4800 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

## Disclaimer Notice

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Rectifier			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$			2300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$			2200	V
$I_{RD}$	reverse current, drain current	$V_{R/D} = 2200\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$		100	$\mu\text{A}$
		$V_{R/D} = 2200\text{ V}$	$T_{VJ} = 140^{\circ}\text{C}$		10	mA
$V_T$	forward voltage drop	$I_T = 75\text{ A}$	$T_{VJ} = 25^{\circ}\text{C}$		1.24	V
		$I_T = 150\text{ A}$			1.51	V
		$I_T = 75\text{ A}$	$T_{VJ} = 125^{\circ}\text{C}$		1.21	V
		$I_T = 150\text{ A}$			1.58	V
$I_{TAV}$	average forward current	$T_C = 85^{\circ}\text{C}$	$T_{VJ} = 140^{\circ}\text{C}$		75	A
$I_{T(RMS)}$	RMS forward current	180° sine			118	A
$V_{T0}$	threshold voltage	} for power loss calculation only	$T_{VJ} = 140^{\circ}\text{C}$		0.84	V
$r_T$	slope resistance				5	m $\Omega$
$R_{thJC}$	thermal resistance junction to case				0.38	K/W
$R_{thCH}$	thermal resistance case to heatsink			0.2		K/W
$P_{tot}$	total power dissipation		$T_C = 25^{\circ}\text{C}$		302	W
$I_{TSM}$	max. forward surge current	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$		1.40	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		1.51	kA
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 140^{\circ}\text{C}$		1.19	kA
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		1.29	kA
$I^2t$	value for fusing	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$		9.80	kA <sup>2</sup> s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		9.49	kA <sup>2</sup> s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 140^{\circ}\text{C}$		7.08	kA <sup>2</sup> s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		6.87	kA <sup>2</sup> s
$C_J$	junction capacitance	$V_R = 700\text{ V}$ $f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}\text{C}$		39	pF
$P_{GM}$	max. gate power dissipation	$t_p = 30\text{ }\mu\text{s}$	$T_C = 140^{\circ}\text{C}$		10	W
		$t_p = 300\text{ }\mu\text{s}$			5	W
$P_{GAV}$	average gate power dissipation				0.5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 140^{\circ}\text{C}; f = 50\text{ Hz}$ repetitive, $I_T = 225\text{ A}$			150	A/ $\mu\text{s}$
		$t_p = 200\text{ }\mu\text{s}; di_G/dt = 0.45\text{ A}/\mu\text{s};$ $I_G = 0.45\text{ A}; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 75\text{ A}$			500	A/ $\mu\text{s}$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty$ ; method 1 (linear voltage rise)	$T_{VJ} = 140^{\circ}\text{C}$		1000	V/ $\mu\text{s}$
$V_{GT}$	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$		1.4	V
			$T_{VJ} = -40^{\circ}\text{C}$		1.6	V
$I_{GT}$	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$		95	mA
			$T_{VJ} = -40^{\circ}\text{C}$		200	mA
$V_{GD}$	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 140^{\circ}\text{C}$		0.2	V
$I_{GD}$	gate non-trigger current				10	mA
$I_L$	latching current	$t_p = 10\text{ }\mu\text{s}$	$T_{VJ} = 25^{\circ}\text{C}$		200	mA
		$I_G = 0.45\text{ A}; di_G/dt = 0.45\text{ A}/\mu\text{s}$				
$I_H$	holding current	$V_D = 6\text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}\text{C}$		200	mA
$t_{gd}$	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}\text{C}$		2	$\mu\text{s}$
		$I_G = 0.45\text{ A}; di_G/dt = 0.45\text{ A}/\mu\text{s}$				
$t_q$	turn-off time	$V_R = 100\text{ V}; I_T = 75\text{ A}; V = \frac{2}{3} V_{DRM}$ $di/dt = 10\text{ A}/\mu\text{s}$ $dv/dt = 20\text{ V}/\mu\text{s}$ $t_p = 200\text{ }\mu\text{s}$	$T_{VJ} = 125^{\circ}\text{C}$		500	$\mu\text{s}$



Package TO-240AA				Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit	
$I_{RMS}$	RMS current	per terminal			200	A	
$T_{VJ}$	virtual junction temperature		-40		140	°C	
$T_{op}$	operation temperature		-40		125	°C	
$T_{stg}$	storage temperature		-40		125	°C	
<b>Weight</b>					81	g	
$M_D$	mounting torque		2.5		4	Nm	
$M_T$	terminal torque		2.5		4	Nm	
$d_{Spp/App}$	creepage distance on surface   striking distance through air	terminal to terminal	13.0	9.7		mm	
$d_{Spb/Apb}$		terminal to backside	16.0	16.0		mm	
$V_{ISOL}$	isolation voltage	t = 1 second	50/60 Hz, RMS; $I_{ISOL} \leq 1$ mA		4800	V	
		t = 1 minute			4000	V	



**Part description**

- M = Module
- C = Thyristor (SCR)
- N = High Voltage Thyristor
- A = ( $\geq 2000V$ )
- 75 = Current Rating [A]
- PD = Phase leg
- 2200 = Reverse Voltage [V]
- TB = TO-240AA-1B

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCNA75PD2200TB	MCNA75PD2200TB	Box	36	520482

**Equivalent Circuits for Simulation**

\* on die level

$T_{VJ} = 140^{\circ}C$



Thyristor

$V_{0\ max}$	threshold voltage	0.84	V
$R_{0\ max}$	slope resistance *	3.7	mΩ



Outlines TO-240AA



General tolerance: DIN ISO 2768 class „c“



Optional accessories for modules

Keyed gate/cathode twin plugs with wire length = 350 mm, gate = white, cathode = red  
Type ZY 200L (L = Left for pin pair 4/5) UL 758, style 3751



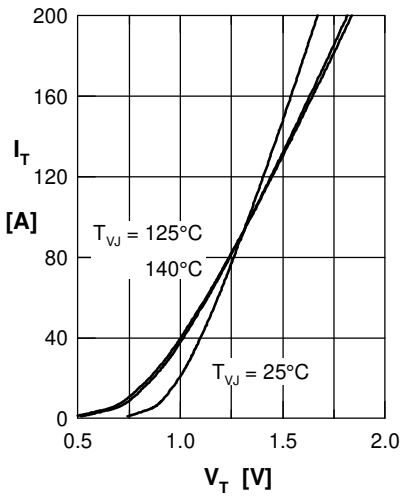
**Thyristor**


Fig. 1 Forward characteristics

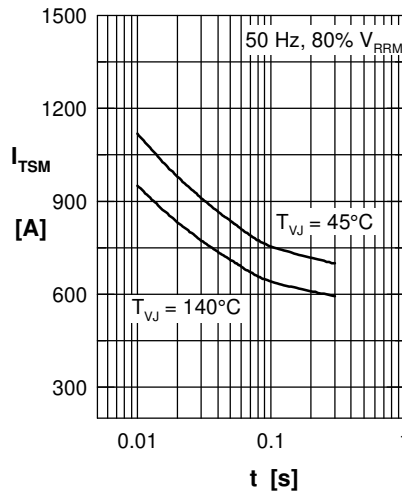
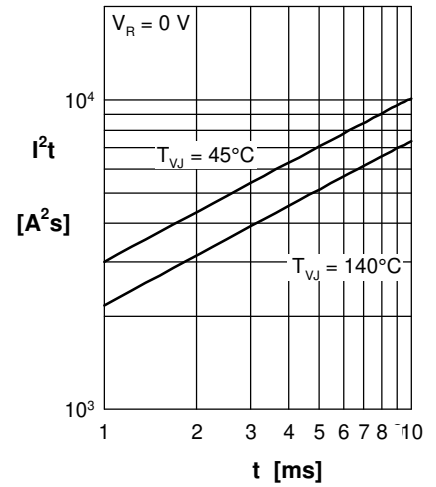
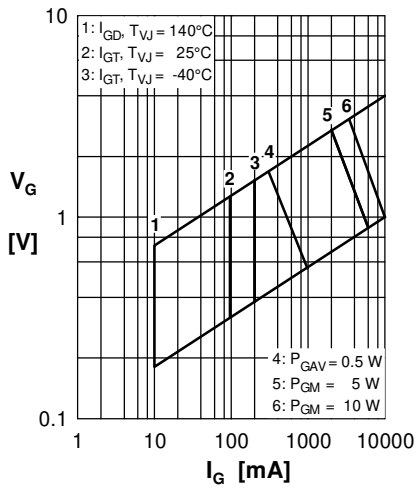

 Fig. 2 Surge overload current  
 $I_{TSM}$ : crest value, t: duration

 Fig. 3  $I^2t$  versus time (1-10 s)


Fig. 4 Gate voltage &amp; gate current

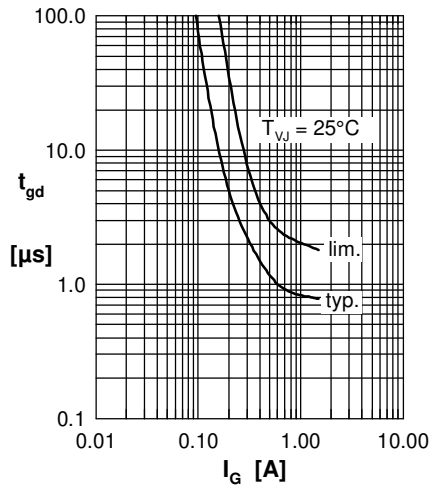
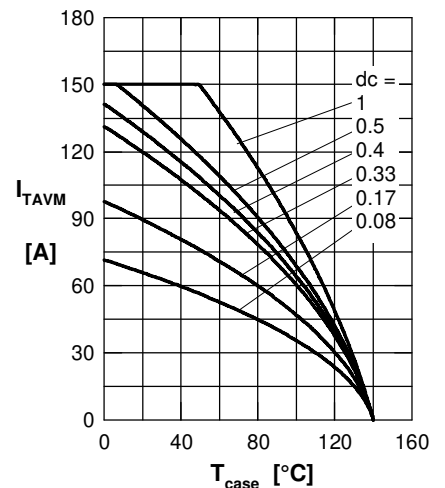

 Fig. 5 Gate controlled delay time  $t_{gd}$ 


Fig. 6 Max. forward current at case temperature

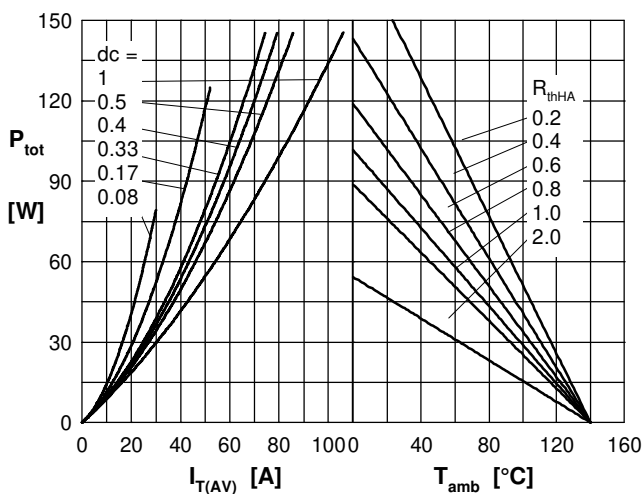
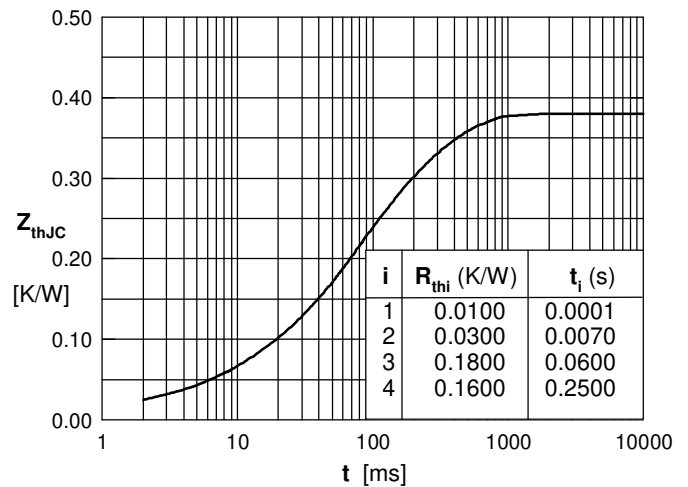

 Fig. 7a Power dissipation versus direct output current  
 Fig. 7b and ambient temperature


Fig. 8 Transient thermal impedance junction to case