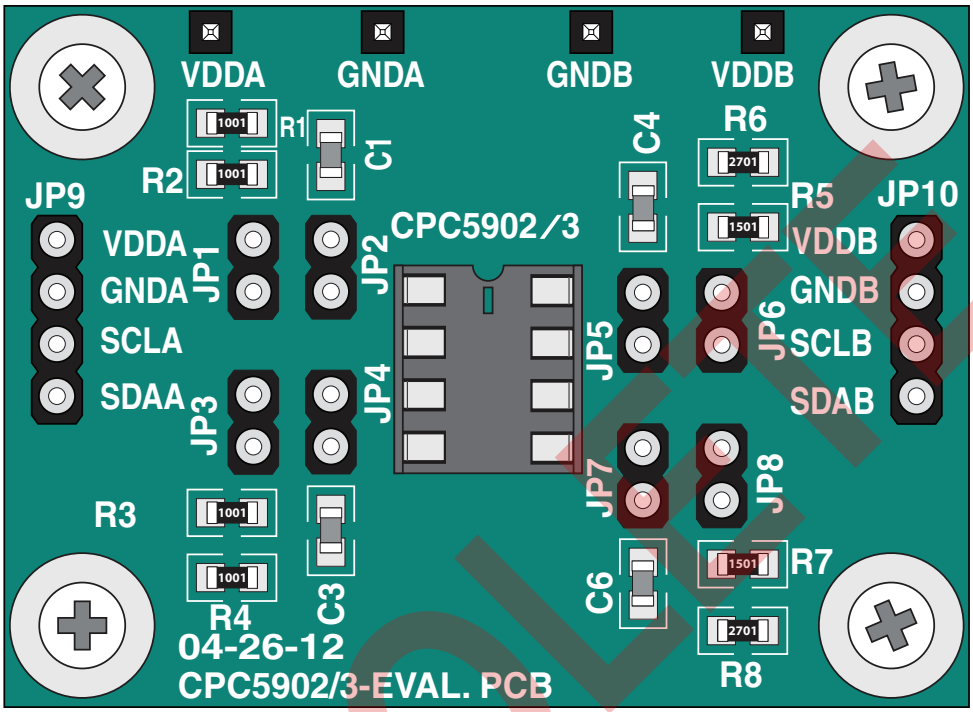
IXYS
INTEGRATED CIRCUITS DIVISION

CPC5902G/CPC5903G Evaluation Board User's Guide



The CPC5902G/5903G Evaluation Board can be used to isolate an I^2C bus, and to evaluate the performance obtainable when communicating between the user's I^2C devices. The 8-pin DIP socket can be populated with either a CPC5902G (for both SCL and SDA bidirectional) or with a CPC5903G (for SDA bidirectional, SCL sideA to sideB only).

At the left side of the board are four 0.1 inch centered posts that carry VDDA, GNDA, SCLA and SDAA. See the drawing above for signal, component, and jumper locations. Best performance will result if the VDDA and GNDA posts are connected to the same VDD and GND as the sideA I^2C bus master. The SCLA post should be connected to the I^2C serial clock line SCL at the bus master on sideA. In addition, the SDAA post should be connected to the I^2C serial data line at the bus master. On the right side of the board there are four posts which carry VDDB, GNDB, SCLB and SDAB when connected to the sideB I^2C devices.

At the top left of the board are duplicate posts, which are electrically shorted to the VDDA and GNDA posts on the left side of the board. These two posts enable convenient operation in standalone mode, when a full I^2C bus may not be available at sideA. Similarly, at the top right of the board, there are duplicates of the VDDB and GNDB posts. The CPC5902G and CPC5903G will each operate correctly for $2.7V < VDDA < 5.5V$ and $2.7V < VDDB < 5.5V$.

While it is possible to attach a second lab power supply to VDDA, which is not identical to the supply at the bus master on sideA, and to operate the board with a live I^2C interface, this is not the recommended mode of operation. The same is true for connecting a second, non-identical lab power supply to VDDB. The V_{IL} and V_{IH} voltages at the bus isolator are derived from the VDDA and VDDB voltages. Thus, the switching thresholds will differ, and noise rejection of the bus will be worse if the voltage at VDDA is not identical to the voltage at the VDD connected to the devices as well as any pull-up resistors on the rest of the sideA bus segment. Similarly, VDDB should be the same voltage used at the devices and any pull-ups on the sideB bus. If either of VDDA or VDDB is not the

same as that used at devices on their buses, the performance of the actual system at power up will not be observable. VDDA does not need to be the same value as VDDB, but, as mentioned above, should be the same voltage as used on the rest of the sideA bus segment.

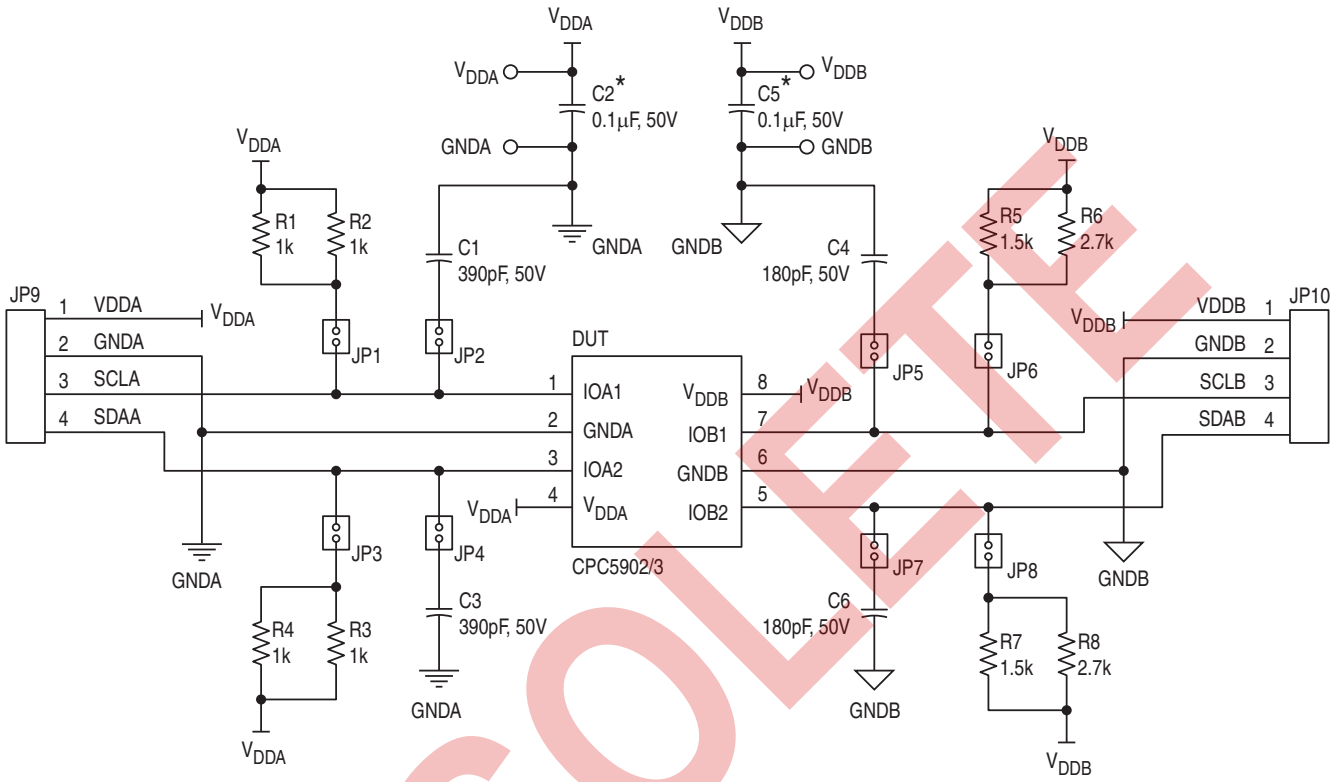
The posts at JP1 on the SCLA line can be used with a 0.1-inch header jumper to add 500Ω (nominal) of pull-up resistance to the SCLA line. Similarly JP3 adds 500Ω of pull-up resistance to the SDAA line. These jumpers are generally not used if there are already minimum value pull-up resistors elsewhere on the bus. For operation at 3.3V at VDDA and a bus driver delivering 0.4V active low, the I_{OL} current will be 2.9V/500Ω = 5.8mA. This is close to the minimum guaranteed value of 6mA for I^2C fast mode. For operation at 5V, this resistance should be increased: 5.0-0.4=4.6V and 4.6V/6mA = 766Ω. The 500Ω has been implemented by using R1=R2=1kΩ in parallel. A quick way to evaluate a 5V system would be to use a soldering iron to remove either R1 or R2 to increase the resistance to 1kΩ; however, slightly faster operation would result from using a pull-up resistor of perhaps 820Ω.

In systems with significant cable length, it is often preferred to split the pull-up resistance by paralleling a physical resistor at both ends of the non-isolated bus segment. To evaluate the performance of a bisected pull-up, a soldering iron can be used to remove either R1 or R2, and a 1kΩ resistor (for a 3.3V system) can be added, if necessary, near the bus master on the sideA bus segment.

The 2 posts at JP2 and JP4 can be jumpered to add 390pF of capacitive load to the SCLA and SDAA lines. These jumpers can be used to load the I^2C lines to I^2C fast mode's worst case: 400pF in standalone mode. The jumpers can also be used to add capacitance to the sideA bus segment if it is extremely lightly loaded, but loading beyond 400pF total does not guarantee operation at 400kHz by the I^2C fast mode specification.

On the right side, the posts at JP5 and JP7 can be used to add 964Ω pull-ups to the SCLB and SDAB lines. For VDDB = 3.3V and V_{OL} = 0.23VDDB=0.76V, this would yield 3.3 - 0.76 = 2.54V across 964Ω, or 2.635mA of output current sunk by the sideB drivers. Other devices on the sideB bus might drive to V_{OL} = 0.4V and sink 3.01mA. The CPC5902G/5903G drivers at sideB are only rated for 3mA when used at VDDB less than 4.5V. The sideB drivers are rated for 6mA operation at up to 5.5V. At 5.5V, they will drive to 0.23*5.5=1.265V and will pull 4.4mA if the pull-up is unchanged. At 5.5V, the pull-up resistor would need to be larger than 705Ω to limit I_{OL} to less than 6mA.

1. Evaluation Board Schematic



*Note: C2 and C5 are located on the bottom side of the board

For additional information please visit www.ixysic.com

Specification: UG-CPC590x_EvalBd-ROBS

6/7/2022