Gating, Latching, and Holding of SCRs and Triacs

Introduction

Gating, latching, and holding currents of Thyristors are some of the most important parameters. These parameters and their interrelationship determine whether the SCRs and Triacs will function properly in various circuit applications.

This application note describes how the SCR and Triac parameters are related. This knowledge helps users select best operating modes for various circuit applications.

Gating of SCRs and Triacs

Three general methods are available to switch Thyristors to on-state condition:

- Applying proper gate signal
- Exceeding Thyristor static dv/dt characteristics
- Exceeding voltage breakover point

This application note examines only the application of proper gate signal. Gate signal must exceed the I_{GT} and V_{GT} requirements of the Thyristor being used. I_{GT} (gate trigger current) is the minimum gate current required to switch a Thyristor from the off state to the on state. V_{GT} (gate trigger voltage) is the voltage required to produce the gate trigger current.

SCRs (unilateral devices) require a positive gate signal with respect to the cathode polarity. Figure AN1002.1 shows the current flow in a cross-sectional view of the SCR chip.

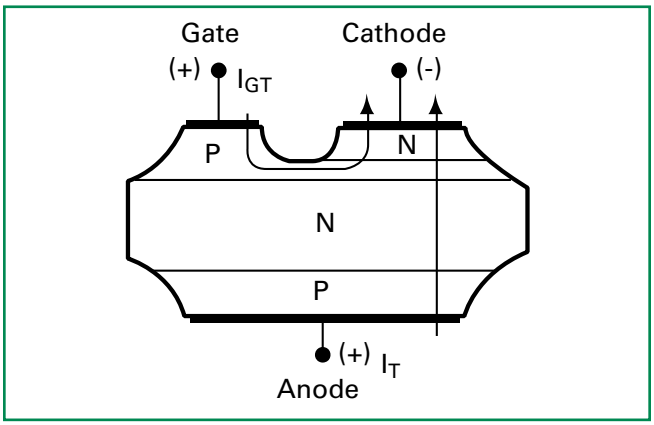

Figure AN1002.1 SCR Current Flow

In order for the SCR to latch on, the anode-to-cathode current (I_T) must exceed the latching current (I_L) requirement. Once latched on, the SCR remains on until it is turned off when anode-to-cathode current drops below holding current (I_H) requirement.

Triacs (bilateral devices) can be gated on with a gate signal of either polarity with respect to the MT1 terminal; however, different polarities have different requirements of I_{GT} and V_{GT}. Figure AN1002.2 illustrates current flow through the Triac chip in various gating modes.

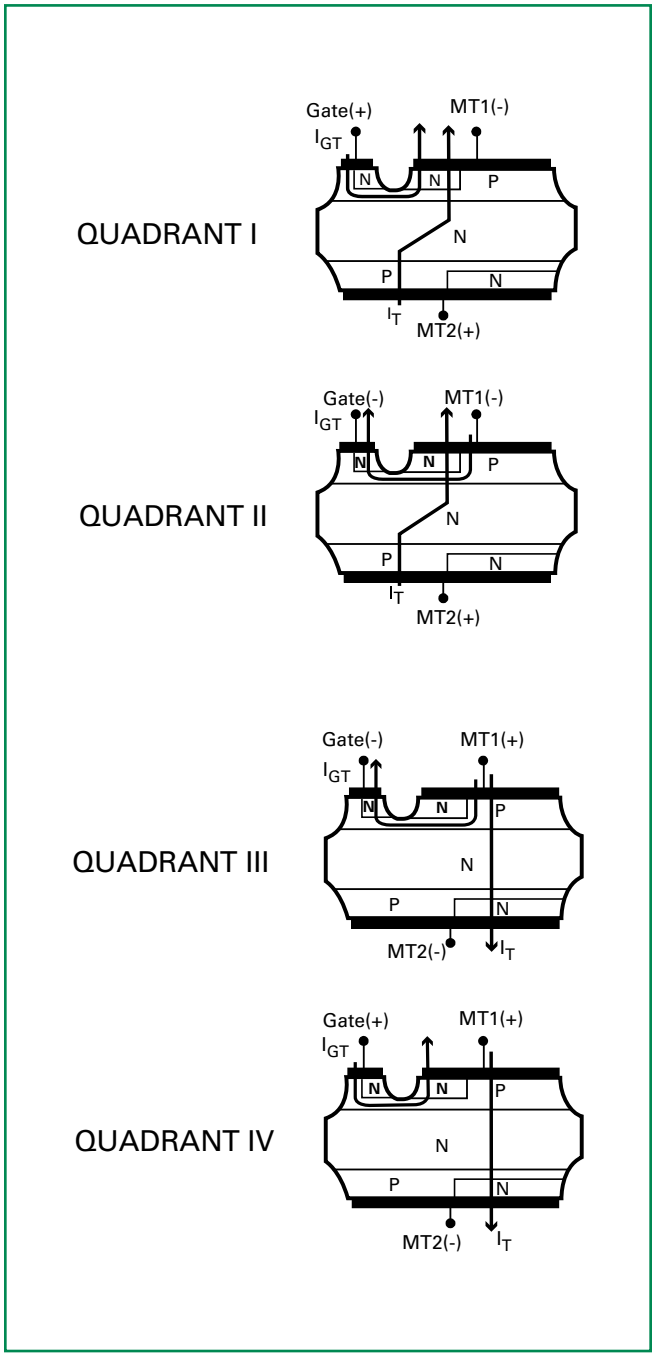

Figure AN1002.2 Triac Current Flow (Four Operating Modes)

Triacs can be gated on in one of four basic gating modes as shown in Figure AN1002.3. The most common quadrants for gating on Triacs are Quadrants I and III, where the gate supply is synchronized with the main terminal supply (gate positive – MT2 positive, gate negative – MT2 negative). Optimum Triac gate sensitivity is achieved when operating in Quadrants I and III due to the inherent Thyristor chip construction. If Quadrants I and III cannot be used, the next best operating modes are Quadrants II and III where the gate supply has a negative polarity with an AC main terminal supply. Typically, Quadrant II is approximately equal in gate sensitivity to Quadrant I; however, latching current sensitivity in Quadrant II is lowest. Therefore, it is difficult for Triacs to latch on in Quadrant II when the main terminal current supply is very low in value.

Special consideration should be given to gating circuit design when Quadrants I and IV are used in actual application, because Quadrant IV has the lowest gate sensitivity of all four operating quadrants.

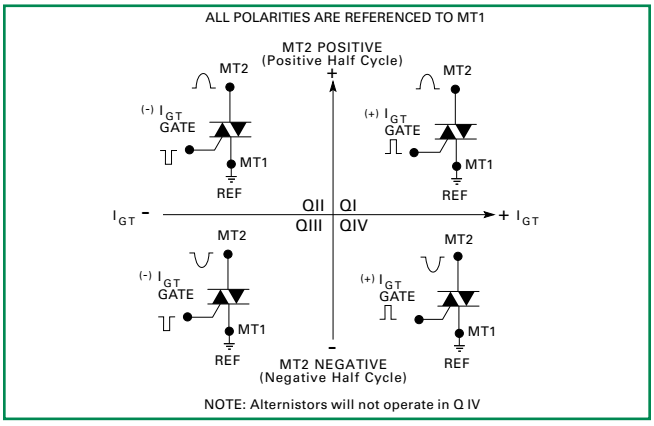

Figure AN1002.3 Definition of Operating Quadrants in Triacs

The following table shows the relationships between different gating modes in current required to gate on Triacs.

Typical Ratio of $\frac{I_{GT}(\text{in given Quadrant})}{I_{GT}(\text{Quadrant 1})}$ at 25°C				
Type	Operating Mode			
	Quadrant I	Quadrant II	Quadrant III	Quadrant IV
4 A Triac	1	1.6	2.5	2.7
10 A Triac	1	1.5	1.4	3.1

Example of 4 A Triac:

If $I_{GT}(I)$ = 10 mA, then

$I_{GT}(II)$ = 16 mA

$I_{GT}(III)$ = 25 mA

$I_{GT}(IV)$ = 27 mA

Gate trigger current is temperature-dependent as shown in Figure AN1002.4. Thyristors become less sensitive with decreasing temperature and more sensitive with increasing temperature.

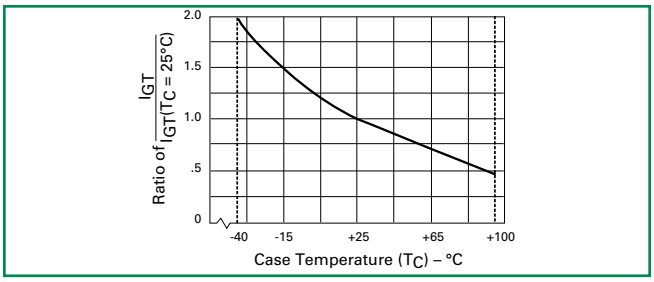

Figure AN1002.4 Typical DC Gate Trigger Current versus Case Temperature

For applications where low temperatures are expected, gate current supply should be increased to at least two to eight times the gate trigger current requirements at 25 °C. The actual factor varies by Thyristor type and the environmental temperature.

Example of a 10 A Triac:

If $I_{GT}(I)$ = 10 mA at 25 °C, then

$I_{GT}(I)$ = 20 mA at -40 °C

In applications where high di/dt, high surge, and fast turn-on are expected, gate drive current should be steep rising (1 µs rise time) and at least twice rated I_{GT} or higher with minimum 3 µs pulse duration. However, if gate drive current magnitude is very high, then duration may have to be limited to keep from overstressing (exceeding the power dissipation limit of) gate junction.

Latching Current of SCRs and Triacs

Latching current (I_L) is the minimum principal current required to maintain the Thyristor in the on state immediately after the switching from off state to on state has occurred and the triggering signal has been removed. Latching current can best be understood by relating to the "pick-up" or "pull-in" level of a mechanical relay. Figure AN1002.5 and Figure AN1002.6 illustrate typical Thyristor latching phenomenon.

In the illustrations in Figure AN1002.5, the Thyristor does not stay on after gate drive is removed due to insufficient available principal current (which is lower than the latching current requirement).

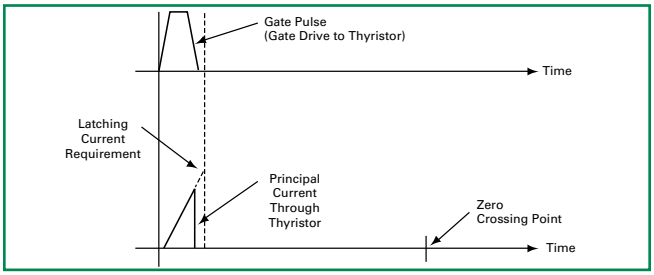

Figure AN1002.5 Latching Characteristic of Thyristor (Device Not Latched)

In the illustration in Figure AN1002.6 the device stays on for the remainder of the half cycle until the principal current falls below the holding current level. Figure AN1002.5 shows the characteristics of the same device if gate drive is removed or shortened before latching current requirement has been met.

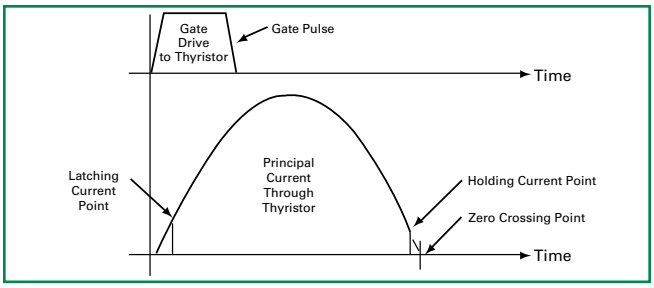

Figure AN1002.6 Latching and Holding Characteristics of Thyristor

Similar to gating, latching current requirements for Triacs are different for each operating mode (quadrant). Definitions of latching modes (quadrants) are the same as gating modes. Therefore, definitions shown in Figure AN1002.2 and Figure AN1002.3 can be used to describe latching modes (quadrants) as well. The following table shows how different latching modes (quadrants) relate to each other. As previously stated, Quadrant II has the lowest latching current sensitivity of all four operating quadrants.

Typical Ratio of $\frac{I_L \text{ (in given Quadrant)}}{I_L \text{(Quadrant 1)}}$ at 25°C				
Type	Operating Mode			
	Quadrant I	Quadrant II	Quadrant III	Quadrant IV
4 A Triac	1	4	1.2	1.1
10 A Triac	1	4	1.1	1

Example of a 4 Amp Triac:

If $I_L(I)$ = 10 mA, then

$I_L(II)$ = 40 mA

$I_L(III)$ = 12 mA

$I_L(IV)$ = 11 mA

Latching current has even somewhat greater temperature dependence compared to the DC gate trigger current. Applications with low temperature requirements should have sufficient principal current (anode current) available to ensure Thyristor latch-on.

Two key test conditions on latching current specifications are gate drive and available principal (anode) current durations. Shortening the gate drive duration can result in higher latching current values.

Holding Current of SCRs and Triacs

Holding current (I_H) is the minimum principal current required to maintain the Thyristor in the on state. Holding current can best be understood by relating it to the "drop-out" or "must release" level of a mechanical relay. Figure AN1002.6 shows the sequences of gate, latching, and holding currents. Holding current will always be less than latching. However, the more sensitive the device, the closer the holding current value approaches its latching current value.

Holding current is independent of gating and latching, but the device must be fully latched on before a holding current limit can be determined.

Holding current modes of the Thyristor are strictly related to the voltage polarity across the main terminals. The following table illustrates how the positive and negative holding current modes of Triacs relate to each other.

Typical Triac Holding Current Ratio		
Type	Operating Mode	
	$I_H(+)$	$I_H(-)$
4 A Triac	1	1.1
10 A Triac	1	1.3

Example of a 10 A Triac:

If $I_H(+)$ = 10 mA, then

$I_H(-)$ = 13 mA

Holding current is also temperature-dependent like gating and latching shown in Figure AN1002.7. The initial on-state current is 200 mA to ensure that the Thyristor is fully latched on prior to holding current measurement. Again, applications with low temperature requirements should have sufficient principal (anode) current available to maintain the Thyristor in the on-state condition.

Both minimum and maximum holding current specifications may be important, depending on application. Maximum holding current must be considered if the Thyristor is to stay in conduction at low principal (anode) current; the minimum holding current must be considered if the device is expected to turn off at a low principal (anode) current.

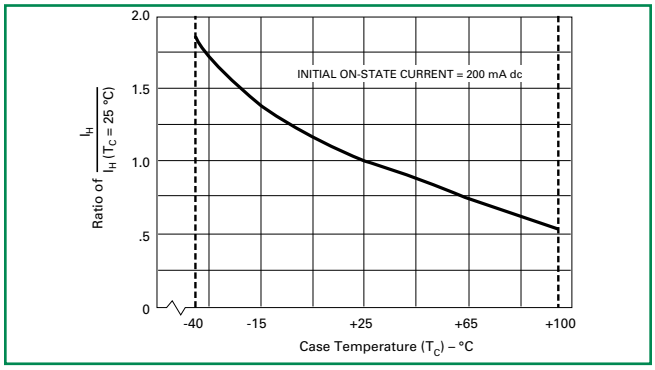

Figure AN1002.7 Typical DC Holding Current vs Case Temperatures

Example of a 10 A Triac:

If $I_H(+)$ = 10 mA at 25 °C, then

$I_H(+) \approx$ 7.5 mA at 65 °C

Relationship of Gating, Latching, and Holding Currents

Although gating, latching, and holding currents are independent of each other in some ways, the parameter values are related. If gating is very sensitive, latching and holding will also be very sensitive and vice versa. One way to obtain a sensitive gate and not-so-sensitive latching-holding characteristic is to have an "amplified gate" as shown in Figure AN1002.8.

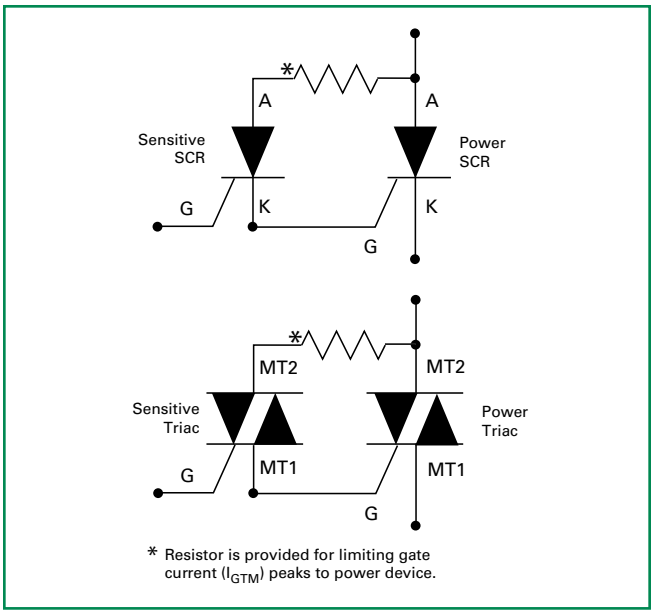

Figure AN1002.8 "Amplified Gate" Thyristor Circuit

The following table and Figure AN1002.9 show the relationship of gating, latching, and holding of a 4 A device.

Typical 4 A Triac Gating, Latching, and Holding Relationship				
Parameter	Quadrants or Operating Mode			
	Quadrant I	Quadrant II	Quadrant III	Quadrant IV
I_{GT} (mA)	10	17	18	27
I_L (mA)	12	48	12	13
I_H (mA)	10	10	12	12

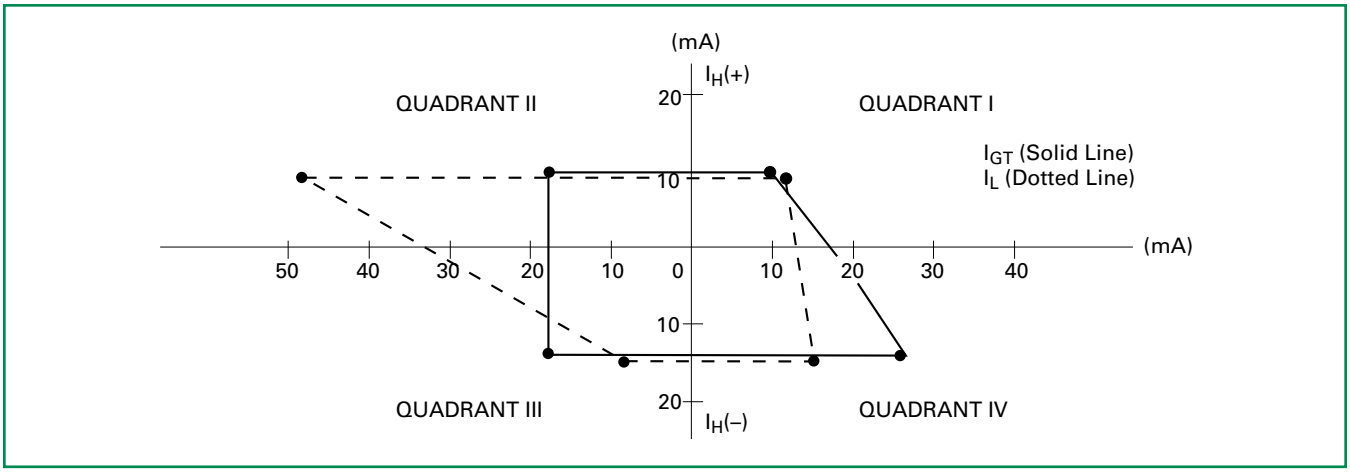

Figure AN1002.9 Typical Gating, Latching, and Holding Relationships of 4 A Triac at 25 °C

The relationships of gating, latching, and holding for several device types are shown in the following table. For convenience all ratios are referenced to Quadrant I gating.

Typical Ratio of Gating, Latching, and Holding Current at 25 °C									
Devices	Ratio								
	$\frac{I_{GT}(II)}{I_{GT}(I)}$	$\frac{I_{GT}(III)}{I_{GT}(I)}$	$\frac{I_{GT}(IV)}{I_{GT}(I)}$	$\frac{I_L(I)}{I_{GT}(I)}$	$\frac{I_L(II)}{I_{GT}(I)}$	$\frac{I_L(III)}{I_{GT}(I)}$	$\frac{I_L(IV)}{I_{GT}(I)}$	$\frac{I_H(+)}{I_{GT}(I)}$	$\frac{I_H(–)}{I_{GT}(I)}$
4A Triac	1.6	2.5	2.7	1.2	4.8	1.2	1.3	1.0	1.2
10A Triac	1.5	1.4	3.1	1.6	4.0	1.8	2.0	1.1	1.6
15A Alternistor	1.5	1.8	–	2.4	7.0	2.1	–	2.2	1.9
1A Sensitive SCR	–	–	–	25	–	–	–	25	–
6A SCR	–	–	–	3.2	–	–	–	2.6	–

Examples of a 10 A Triac:

If I_{GT}(I) = 10 mA, then
I_{GT}(II) = 15 mA
I_{GT}(III) = 14 mA
I_{GT}(IV) = 31 mA

If I_L(I) = 16 mA, then
I_L(II) = 40 mA
I_L(III) = 18 mA
I_L(IV) = 20 mA

If I_H(+) = 11 mA at 25 °C, then
I_H(+) = 16 mA

Summary

Gating, latching, and holding current characteristics of Thyristors are quite important yet predictable (once a single parameter value is known). Their interrelationships (ratios) can also be used to help designers in both initial circuit application design as well as device selection.