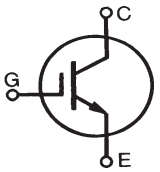
IXYS

GenX3™ 600V IGBT

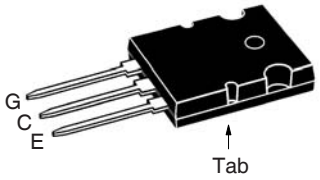
IXGK320N60A3
IXGX320N60A3

V_{CES} = 600V
I_{C110} = 210A
$V_{CE(sat)} \leq$ 1.30V

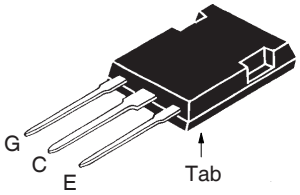
Ultra-Low Vsat PT IGBTs for
up to 5kHz Switching



TO-264 (IXGK)



PLUS247 (IXGX)



G = Gate E = Emitter
C = Collector Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	600	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	600	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C (Chip Capability)	320	A
I_{C110}	T_C = 110°C	210	A
I_{LRMS}	Terminal Current Limit	160	A
I_{CM}	T_C = 25°C, 1ms	700	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 1Ω Clamped Inductive Load	I_{CM} = 320 @ 0.8 • V_{CES}	A
P_C	T_C = 25°C	1000	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
M_d	Mounting Torque (IXGK)	1.13/10	Nm/lb.in
F_C	Mounting Force (IXGX)	20..120/4.5..27	N/lb
Weight	TO-264	10	g
	PLUS247	6	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 1mA, V_{GE} = 0V	600			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	3.0		5.5	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			150	µA
	T_J = 125°C			1.5	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±400	nA
$V_{CE(sat)}$	I_C = 100A, V_{GE} = 15V, Note 1		1.05	1.30	V
	I_C = 320A		1.46		V

Features

- Optimized for Low Conduction Losses
- High Avalanche Capability
- International Standard Packages

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

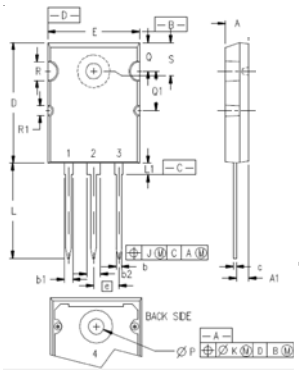
- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts
- Inrush Current Protection Circuits

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Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 60A, V_{CE} = 10V, Note 1	75	125		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1 MHz		18		nF
C_{oes}			985		pF
C_{res}			150		pF
$Q_{g(on)}$	I_C = 80A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		560		nC
Q_{ge}			94		nC
Q_{gc}			195		nC
$t_{d(on)}$	**Resistive load, T_J = 25°C**		63		ns
t_r	I_C = 80A, V_{GE} = 15V		68		ns
$t_{d(off)}$	V_{CE} = 400V, R_G = 1Ω		290		ns
t_f			740		ns
$t_{d(on)}$	**Resistive load, T_J = 125°C**		62		ns
t_r	I_C = 80A, V_{GE} = 15V		77		ns
$t_{d(off)}$	V_{CE} = 400V, R_G = 1Ω		330		ns
t_f			1540		ns
R_{thJC}				0.125	°C/W
R_{thCK}			0.15		°C/W

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

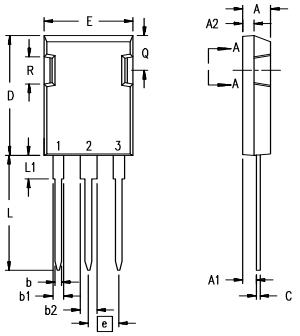
TO-264 Outline



Terminals: 1 - Gate 2, 4 - Collector
3 - Emitter

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
ØP	.122	.138	3.10	3.51
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
ØR	.155	.187	3.94	4.75
ØR1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

PLUS247™ Outline



Terminals: 1 - Gate
2 - Collector
3 - Emitter

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Extended Output Characteristics @ T_J = 25ºC

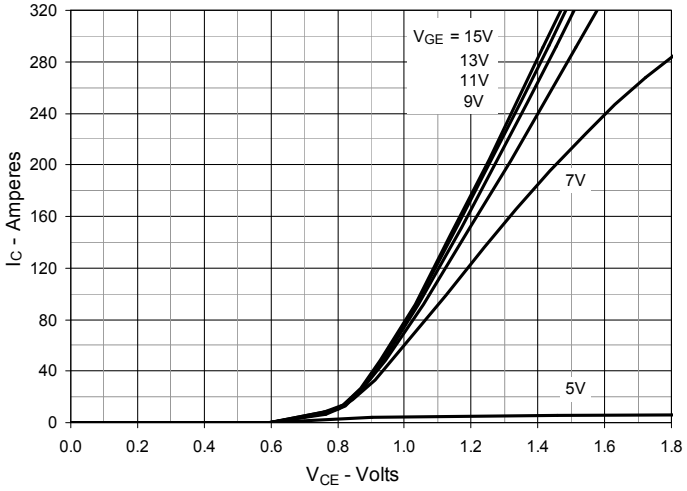


Fig. 2. Output Characteristics @ T_J = 125ºC

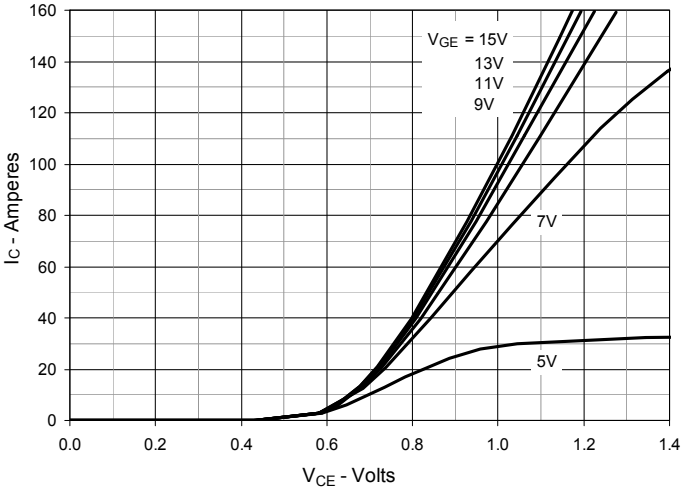


Fig. 3. Dependence of $V_{CE(sat)}$ on Junction Temperature

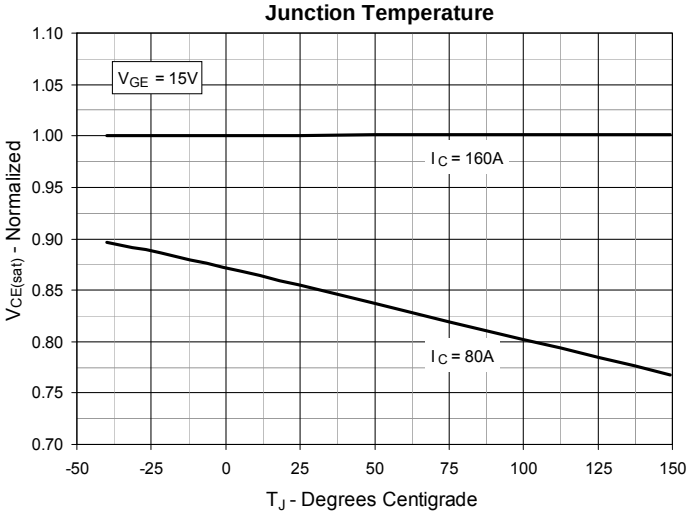


Fig. 4. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

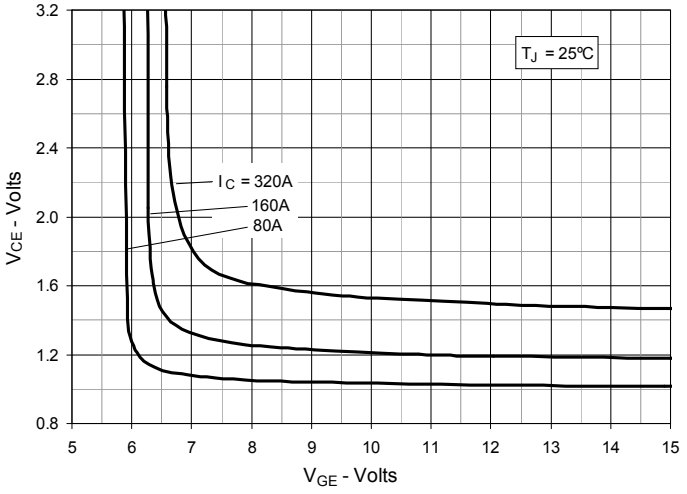


Fig. 5. Input Admittance

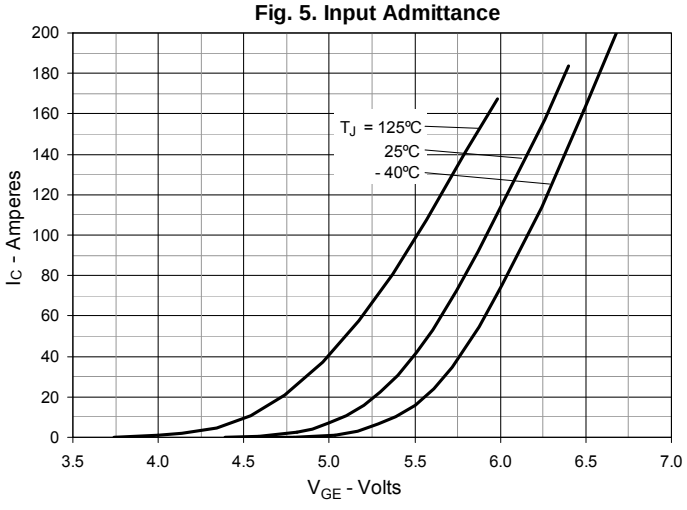
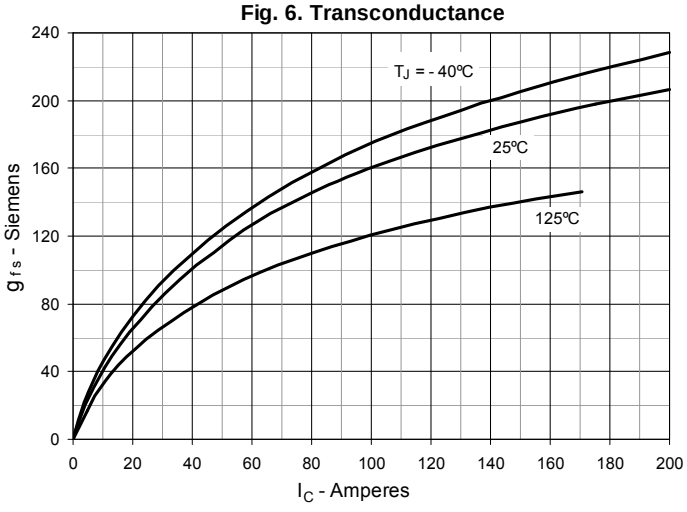


Fig. 6. Transconductance



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Fig. 7. Gate Charge

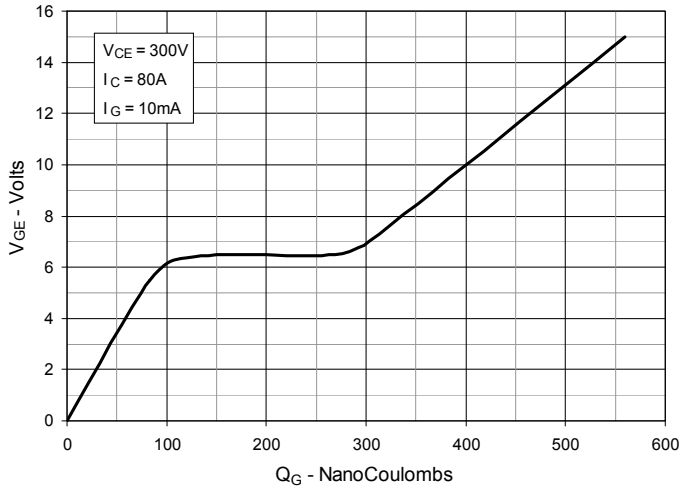


Fig. 8. Capacitance

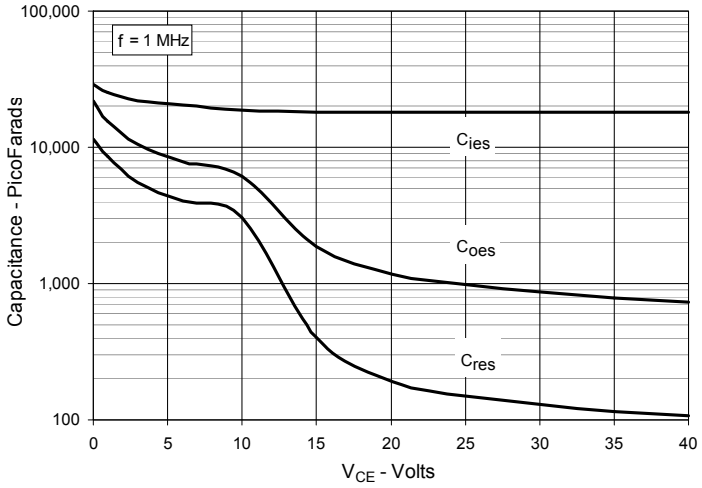


Fig. 9. Reverse-Bias Safe Operating Area

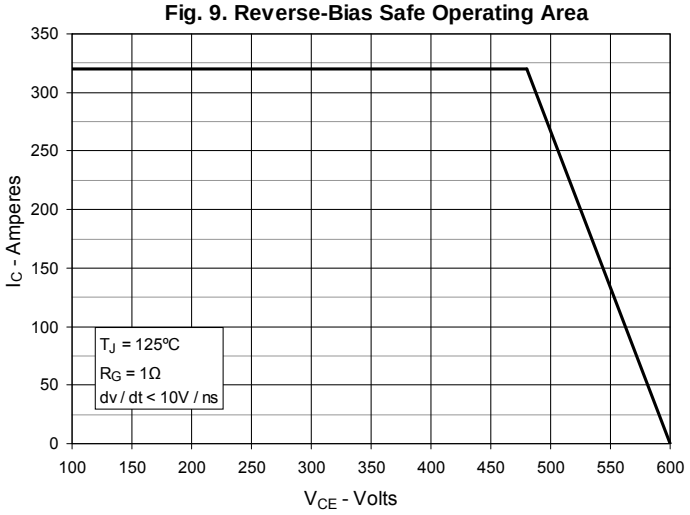


Fig. 10. Maximum Transient Thermal Impedance

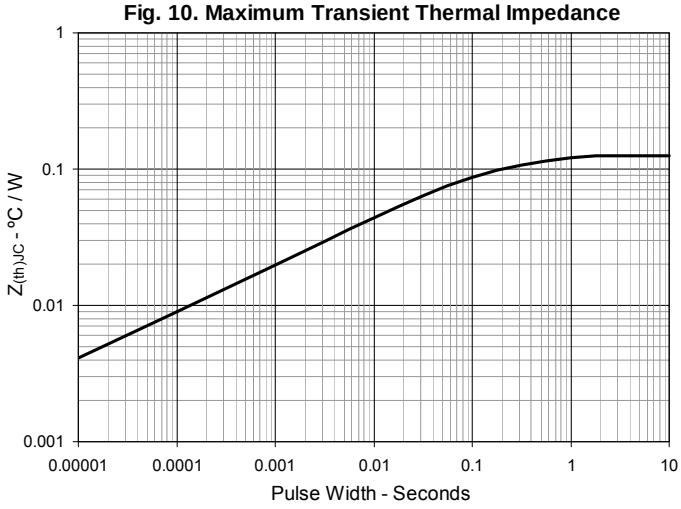


Fig.11. Resistive Turn-on Rise Time vs. Junction Temperature

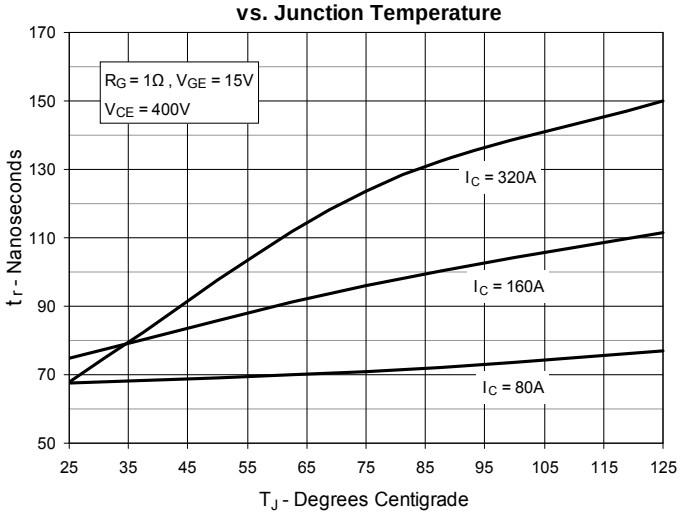


Fig. 12. Resistive Turn-on Rise Time vs. Collector Current

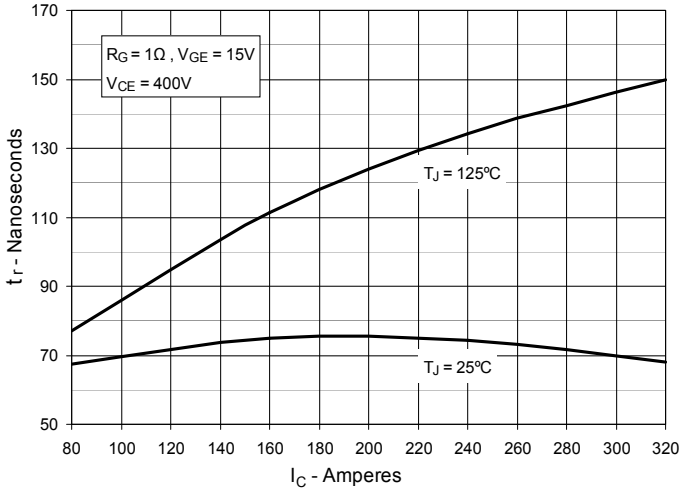


Fig. 13. Resistive Turn-on Switching Times vs. Gate Resistance

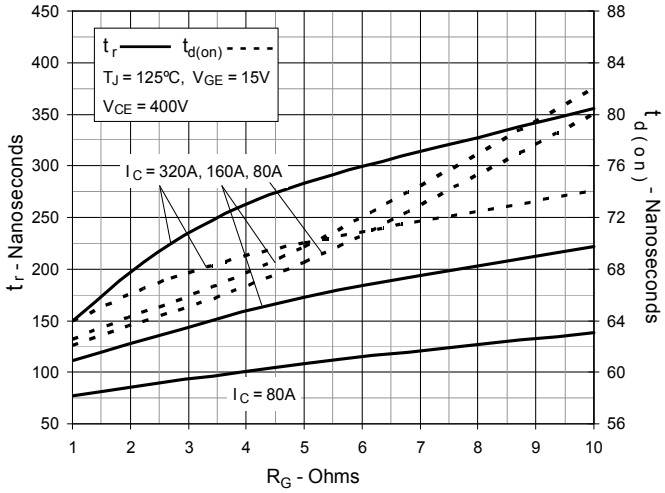


Fig. 14. Resistive Turn-off Switching Times vs. Junction Temperature

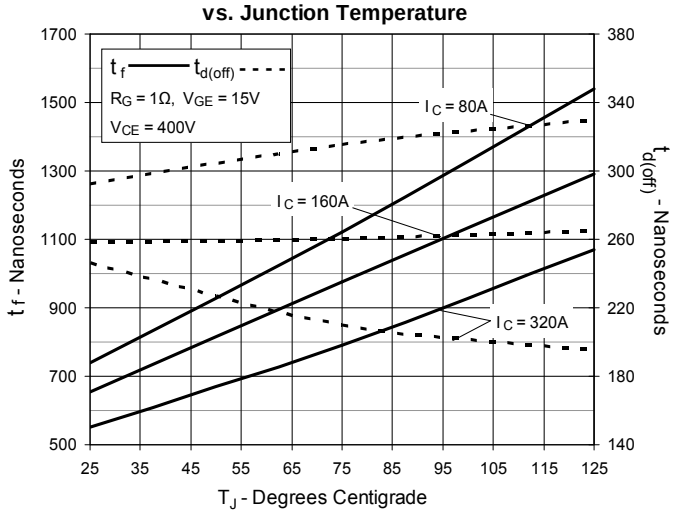


Fig. 15. Resistive Turn-off Switching Times vs. Collector Current

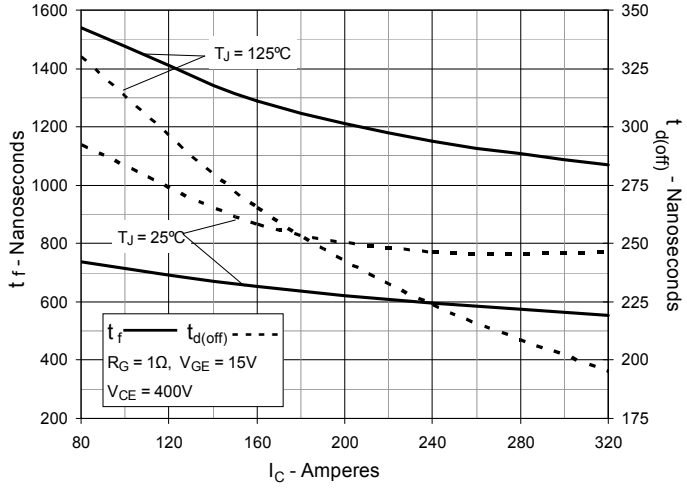
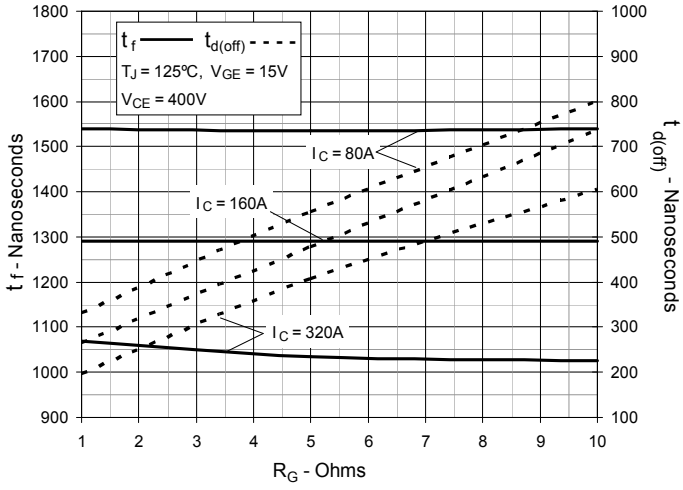


Fig. 16. Resistive Turn-off Switching Times vs. Gate Resistance



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