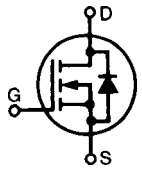
IXYS

HiPerFET™ Power MOSFETs

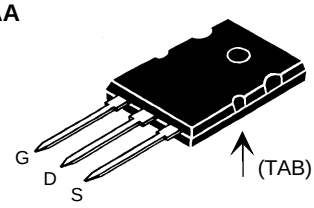
	V_{DSS}	I_{D25}	$R_{DS(on)}$
IXFK72N20	**200 V**	**72 A**	**35 mΩ**
IXFK80N20	**200 V**	**80 A**	**30 mΩ**
	$t_{rr} \leq$ **200 ns**		

N-Channel Enhancement Mode
Avalanche Rated, High dv/dt, Low t_{rr}

Preliminary data



TO-264 AA



G = Gate D = Drain
S = Source TAB = Drain

Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		200	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		200	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	72N20	72	A
		80N20	80	A
I_{DM}	T_C = 25°C,	72N20	288	A
	pulse width limited by T_{JM}	80N20	320	A
I_{AR}	T_C = 25°C		74	A
E_{AR}	T_C = 25°C		45	mJ
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \leq V_{DSS}$, $T_J \leq 150°C$, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		360	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.063 in) from case for 10 s		300 -	°C
M_d	Mounting torque		0.9/6	Nm/lb.in.
Weight			10	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 1 mA		200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA		2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$	T_J = 25°C			200	μA
	V_{GS} = 0 V	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \cdot I_{D25}$	72N20			35	mΩ
		80N20			30	mΩ
	Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %					

Features

- International standard packages
- Molding epoxies meet UL 94 V-0 flammability classification
- Low $R_{DS(on)}$ HDMOS™ process
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic rectifier

Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls

Advantages

- Easy to mount
- Space savings
- High power density

IXYS reserves the right to change limits, test conditions, and dimensions.

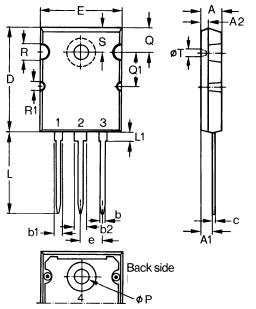
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Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 0.5 • I_{D25}, pulse test	35	42		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		5900		pF
C_{oss}			1140		pF
C_{rss}			480		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25} R_G = (External),		40		ns
t_r			55		ns
$t_{d(off)}$			120		ns
t_f			26		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		280		nC
Q_{gs}			39		nC
Q_{gd}			120		nC
R_{thJC}				0.35	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)		min.	typ.	max.	
I_S	V_{GS} = 0 V	72N20			72	A
		80N20			80	A
I_{SM}	Repetitive; pulse width limited by T_{JM}	72N20			288	A
		80N20			320	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				1.5	V
t_{rr}	I_F = I_S, -di/dt = 100 A/µs, V_R = 100 V				200	ns
Q_{RM}				1.2		µC
I_{RM}				10		A

TO-264 AA Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

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IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents:
4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

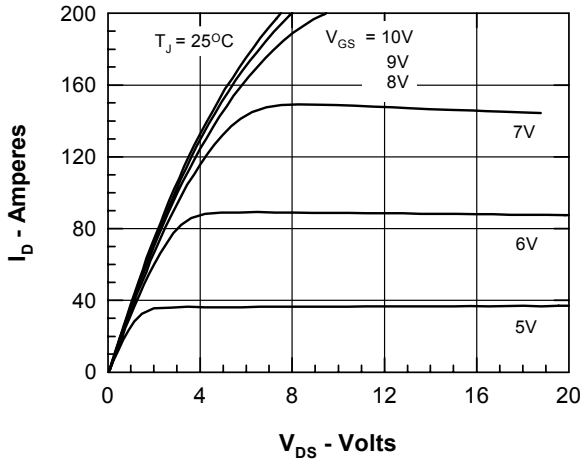


Figure 1. Output Characteristics at 25°C

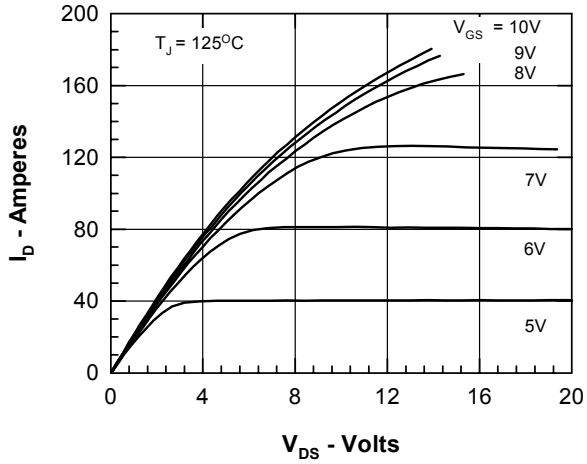


Figure 2. Output Characteristics at 125°C

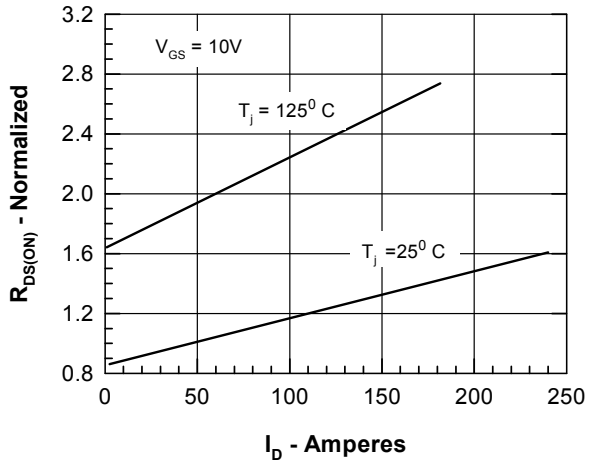


Figure 3. $R_{DS(on)}$ normalized to 0.5 I_{D25} value

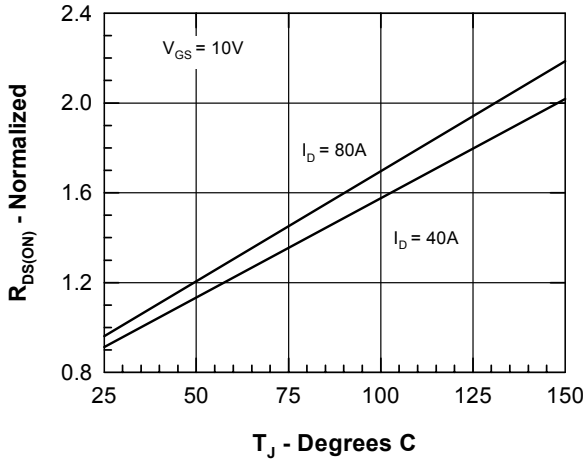


Figure 4. $R_{DS(on)}$ normalized to 0.5 I_{D25} value

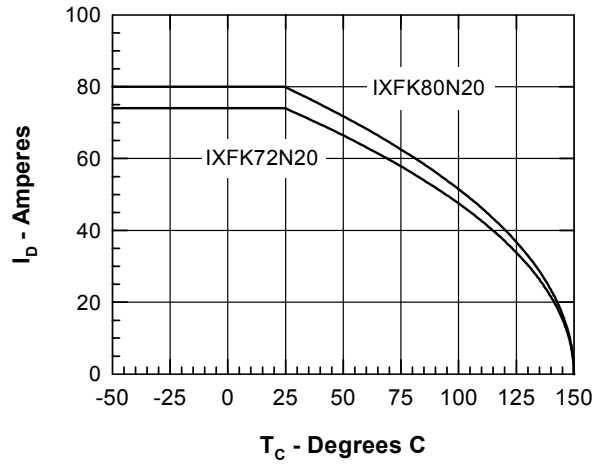


Figure 5. Drain Current vs. Case Temperature

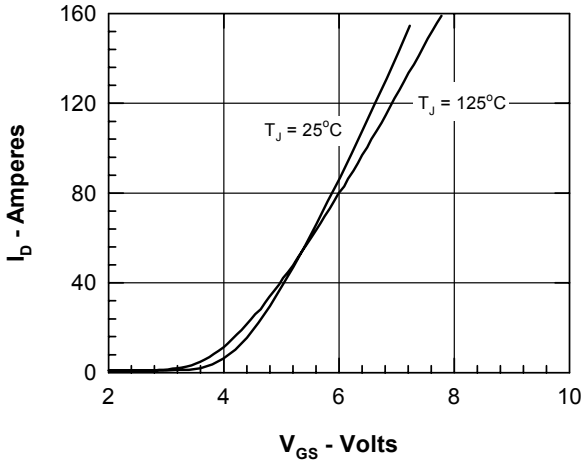


Figure 6. Admittance Curves

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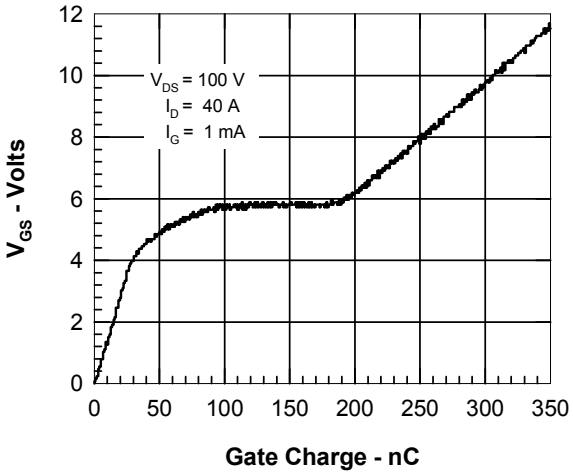


Figure 7. Gate Charge

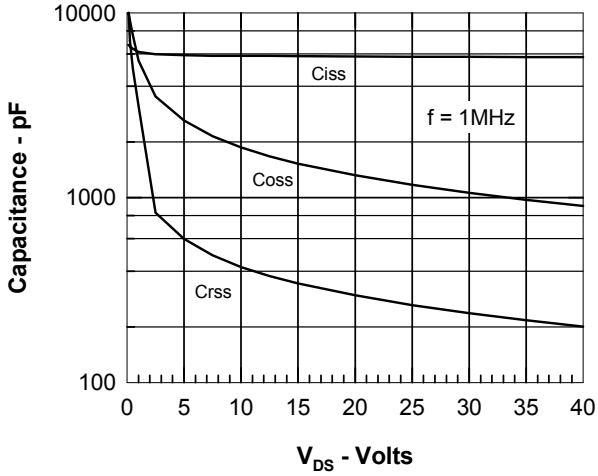


Figure 8. Capacitance Curves

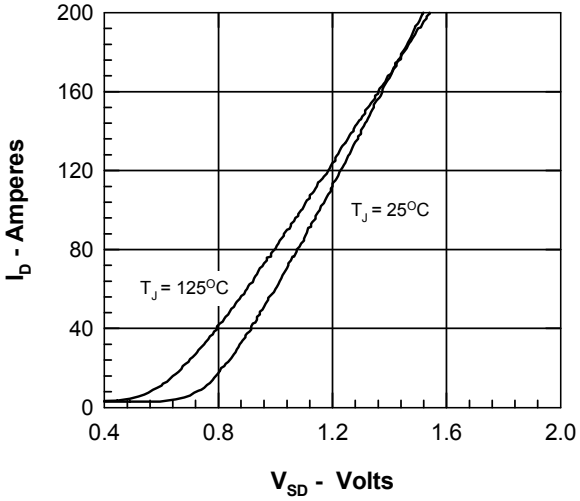


Figure 9. Source Current vs. Source to Drain Voltage

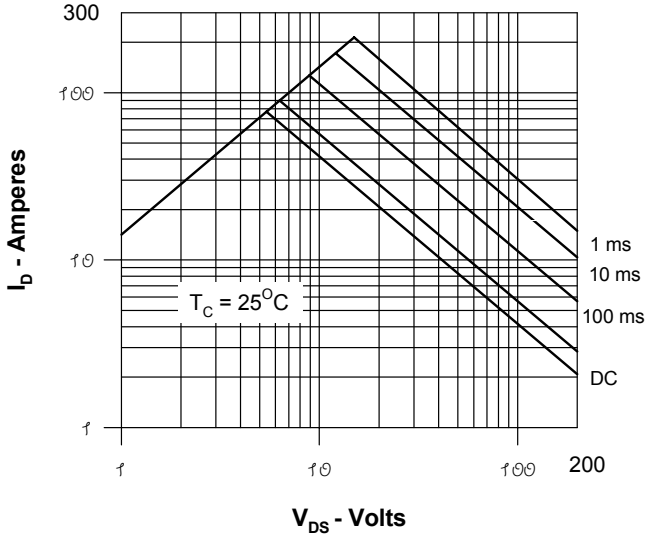


Figure10. Forward Bias Safe Operating Area

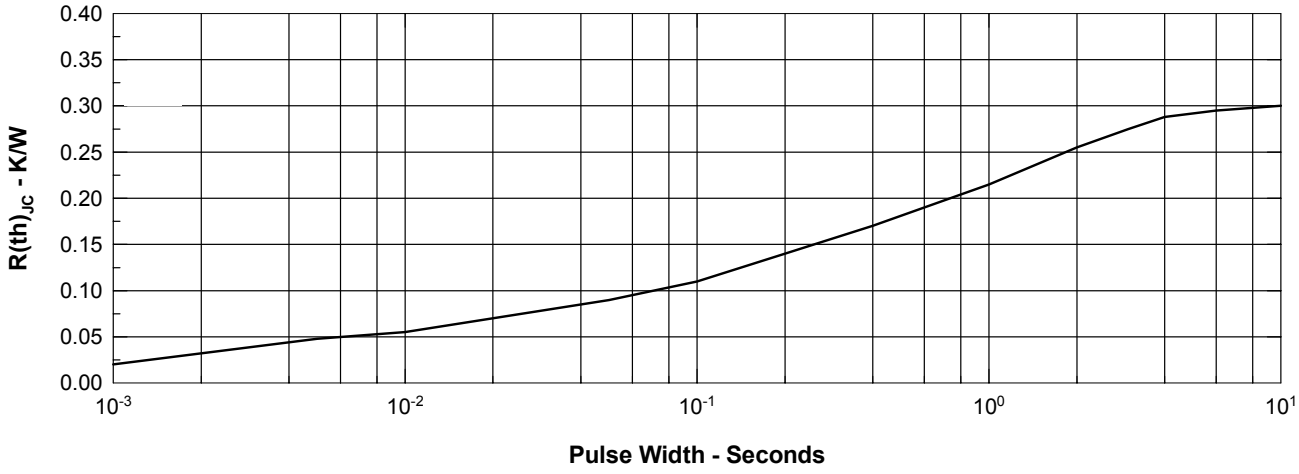


Figure 11. Transient Thermal Resistance

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