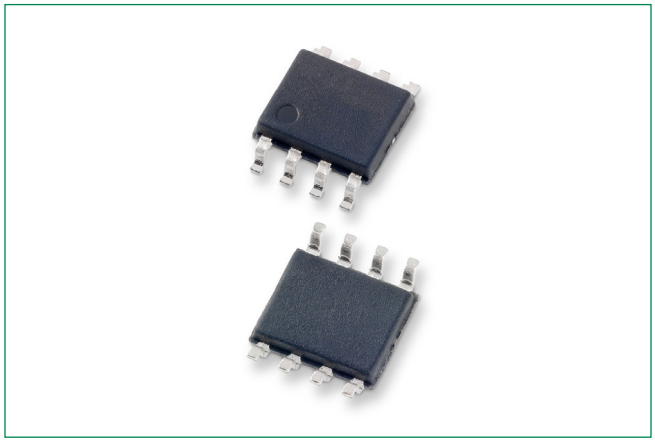
SP725 Series
5pF 8kV Diode Array

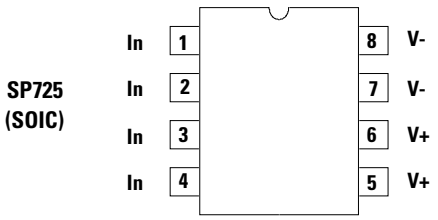
RoHS Pb GREEN



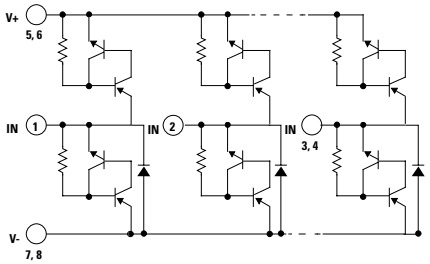
Additional Information

Resources | Accessories | Samples

Pinout



Functional Block Diagram



Description

The SP725 is an array of SCR/Diode bipolar structures for ESD and overvoltage protection of sensitive input circuits. The SP725 has 2 protection SCR/Diode device structures per input. There are a total of 4 available inputs that can be used to protect up to 4 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 4) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one +VBE diode threshold above V+ (Pin 5,6) or one –VBE diode threshold below V- (Pin 7,8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one VBE above V+. A similar clamp to V- is activated if a negative pulse, one VBE less than V-, is applied to an IN input.

Refer to Fig 1 and Table 1 for further details. Refer to Application Note AN9304 and AN9612 for further detail.

Features & Benefits

- ESD Interface per HBM Standards
  - IEC 61000-4-2, Direct Discharge 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge 15kV (Level 4)
  - MIL-STD-3015.7 25kV
- Peak Current Capability
  - IEC 61000-4-5 8/20 µs Peak Pulse Current ± 14 A
  - Single Transient Pulse, 100 µs Pulse Width ± 8 A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to +30V
  - Differential Voltage Range to ±15V
- Fast Switching 2ns Risetime
- Low Input Leakages 5 nA at 25 °C Typical
- Low Input Capacitance 5 pF Typical
- An Array of 4 SCR/Diode Pairs
- Operating Temperature Range -40 °C to 105 °C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

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Revised: GD. 09/07/22

SP725 Series
5pF 8kV Diode Array

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC} , I_{IN} to GND (Refer to Figure 5)	± 8, 100 µs	A
Peak Pulse Current, 8/20µs	± 14	A
ESD Ratings and Capability (Figure 1, Table 1) Load Dump and Reverse Battery (Note 2)		

Caution: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
SOIC Package	170	°C/W
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s) (SOIC - Lead Tips Only)	260	°C

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

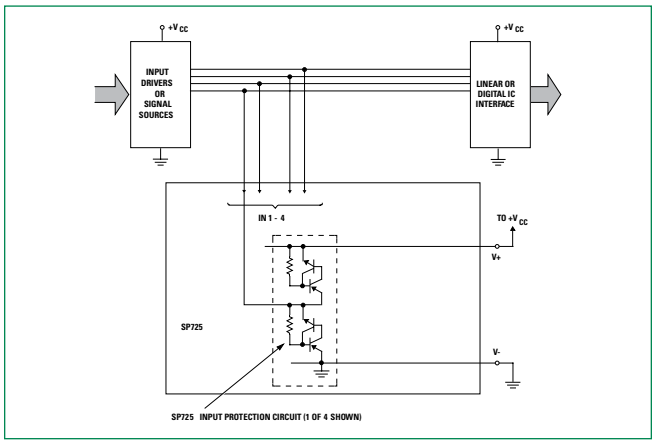
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop		I_{IN} = 2A (Peak Pulse)				
IN to V-	V_{FWDL}		-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		(Note 3)	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} ; (Note 3)	-	0.5	-	Ω
Input Capacitance	C_{IN}			5	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air
2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP725 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance." These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

Typical Application of the SP725

(Application as an Input Clamp for Overvoltage, Greater than 1VBE Above V+ or less than -1VBE below V-)



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5pF 8kV Diode Array

ESD Capability

ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

The SP725 has a Level 4 HBM capability when tested as a device to the IEC 61000-4-2 standard. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "incircuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP725 ESD capability is typically greater than 25kV from 100pF through 1.5kΩ . By strict definition of MIL-STD-3015.7 using "pinto-pin" device testing, the ESD voltage capability is greater than 10kV.

For the SP725 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 2kV from 200pF with no series resistance.

Figure 1:
Electrostatic Discharge Test

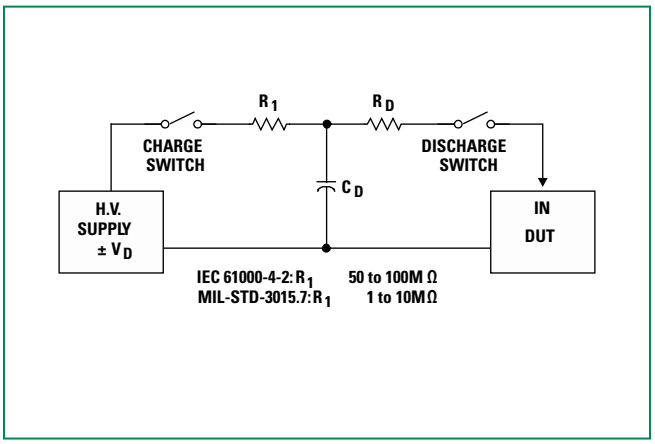


Table 1:
ESD Test Conditions

Standard	Type/Mode	R_D	C_D	$\pm V_D$
IEC 61000-4-2 (Level 4)	HBM, Air Discharge	330 Ω	150pF	15kV
	HBM, Direct Discharge	330 Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5k Ω	100pF	25kV
	Standard HBM	1.5k Ω	100pF	10kV
EIAJ IC121	Machine Model	0k Ω	200pF	2kV

Figure 2:
Low Current SCR Forward Voltage Drop Curve

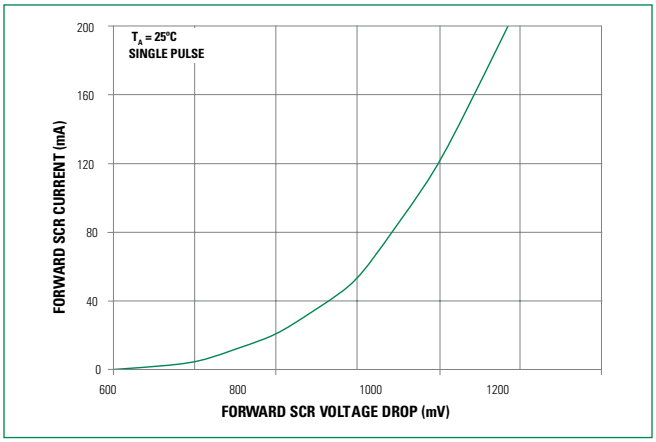
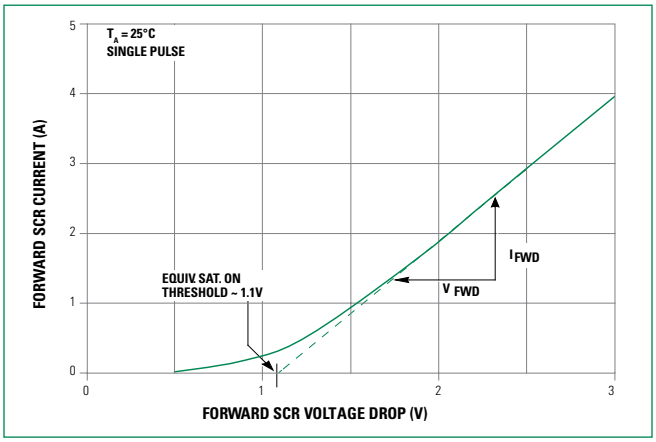


Figure 3:
High Current SCR Forward Voltage Drop Curve



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SP725 Series
5pF 8kV Diode Array

Peak Transient Current Capability for Long Duration Surges

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP725 's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 4.

The test circuit of Figure 4 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP725 'IN' input pin and the (+) current pulse input goes to the SP725 V- pin. The V+ to V- supply of the SP725 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 5 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25 ° C and 105 ° C and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 5.

Note that adjacent input pins of the SP725 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

Figure 4:
Typical SP725 Peak Current Test Circuit with a Variable Pulse Width Input

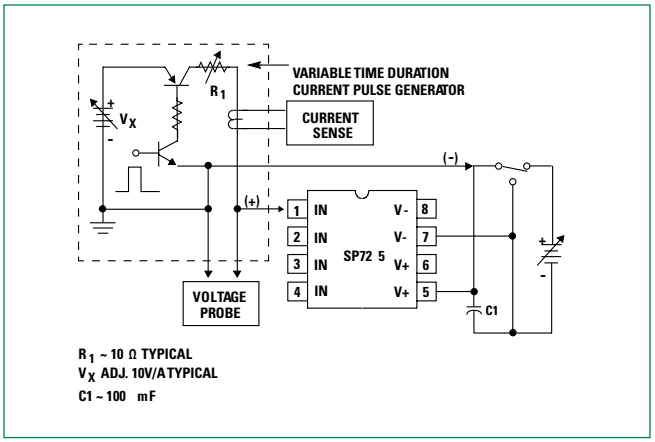
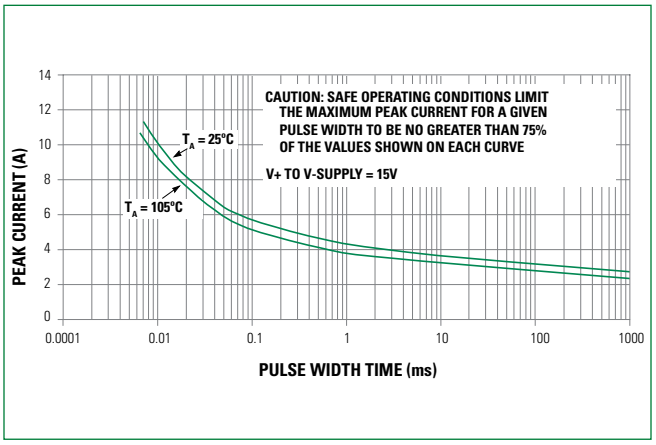


Figure 5:
SP725 Typical Nonrepetitive Peak Current Pulse Capability

Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds

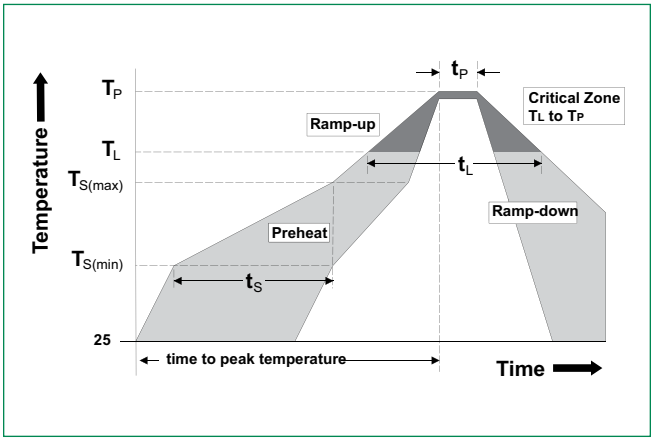


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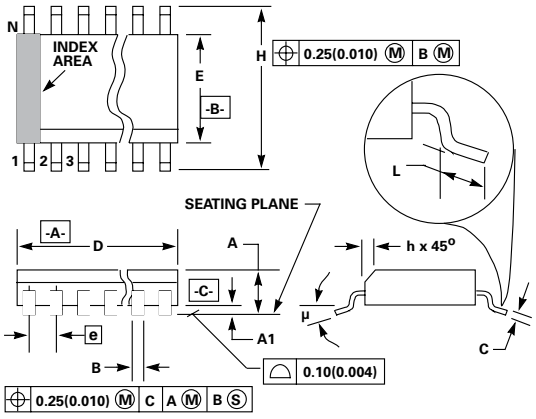
SP725 Series
5pF 8kV Diode Array

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	**- Temperature Min ($T_{s(min)}$)**	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	**- Temperature (T_L) (Liquidus)**	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — Small Outline Plastic Packages (SOIC)



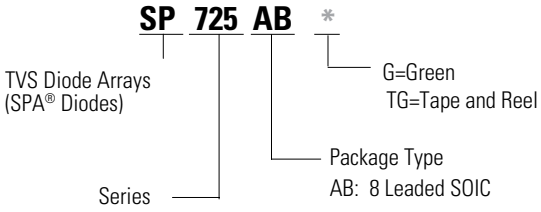
Package	SOIC				
Pins	8				
JEDEC	MS-012				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.35	1.75	0.0532	0.0688	-
A1	0.10	0.25	0.0040	0.0098	-
B	0.33	0.51	0.013	0.020	9
C	0.19	0.25	0.0075	0.0098	-
D	4.80	5.00	0.1890	0.1968	3
E	3.80	4.00	0.1497	0.1574	4
e	1.27 BSC		0.050 BSC		-
H	5.80	6.20	0.2284	0.2440	-
h	0.25	0.50	0.0099	0.0196	5
L	0.40	1.27	0.016	0.050	6
N	8		8		7
μ	0°	8°	0°	8°	-

Notes:
1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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SP725 Series
5pF 8kV Diode Array

Part Numbering System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Substitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

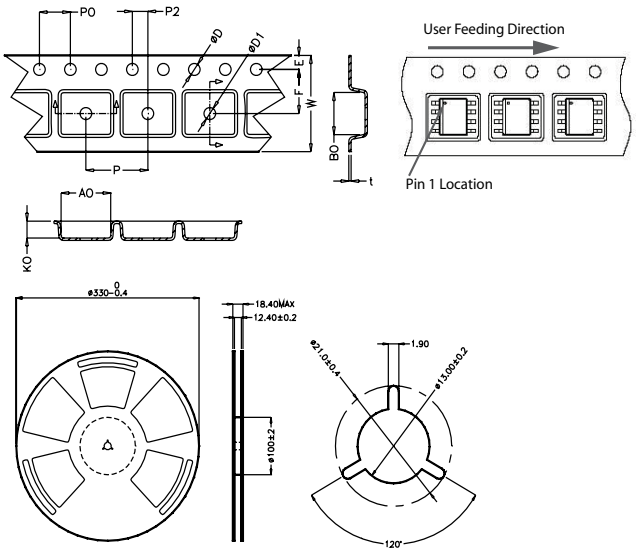
Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4.Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Temp. Range (°C)	Package	Marking	Min. Order Qty.
SP725ABG	-40 to 105	8 Ld SOIC	SP725AB(T)G [1]	1960
SP725ABTG	-40 to 105	8 Ld SOIC Tape and Reel	SP725AB(T)G [1]	2500

Notes:
1. SP725AB(T)G means device marking either SP725ABG or SP725ABTG.

Embossed Carrier Tape & Reel Specification - SOIC Package



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 ± 0.20		1.574 ± 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 ± 0.05		0.012 ± 0.002	

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