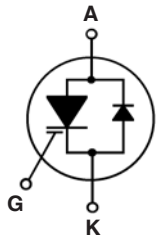
IXYS

Preliminary Technical Information

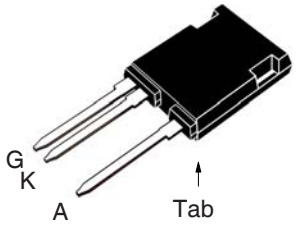
1500V MOS Gated Thyristor w/ Anti-Parallel Diode

IXHX40N150V1HV

V_{DM} = 1500V



TO-247PLUS-HV



G = Gate K = Cathode
A = Anode Tab = Anode

Symbol	Test Conditions	Maximum Ratings	
V_{DM}	T_J = 25°C to 150°C	1500	V
V_{GK}	Continuous	±30	V
V_{GK}	Transient	±40	V
I_{TSM}	T_C = 25°C, 1µs	7.6	kA
	T_C = 25°C, 10µs	3.5	kA
P_D	T_C = 25°C	695	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10s	260	°C
F_C	Mounting Force	20..120 /4.5..27	N/lb
Weight		6	g

Features

- Very High Voltage Package
- Anti-Parallel Diode
- Very High Current Capability

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

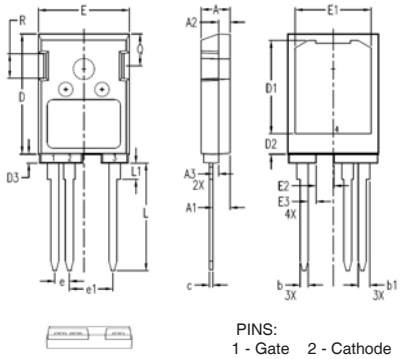
- Capacitive Discharge Circuits
- Ignition Circuits
- Solid State Surge Protection

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
V_{BR}	I_A = 250µA, V_{GK} = 0V	1500			V
$V_{GK(th)}$	I_A = 250µA, V_{AK} = V_{GK}	2.5		5.0	V
V_T	I_T = 1000A, V_{GK} = 15V		5.95	7.5	V
r_T	I_T > I_L, V_{GK} = 15V		1.20		mΩ
V_{BO}	V_{GK} = 15V		6.45		V
I_D	V_{AK} = 1500V, V_{GK} = 0V			15	µA
	T_J = 125°C			1.5	mA
I_L			250		A
I_H			200		A
I_{GKS}	V_{AK} = 0V, V_{GK} = ±30V			±200	nA

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Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
C_{iks}	V_{AK} = 25V, V_{GK} = 0V, f = 1MHz		2825		pF
C_{oks}			164		pF
C_{rks}			50		pF
$Q_{g(on)}$	I_C = 40A, V_{GK} = 15V, V_{AK} = 600V		99		nC
Q_{gk}			22		nC
Q_{ga}			36		nC
t_{ri}	**Capacitive Discharge, T_J = 25°C**		100		ns
t_d	I_A = 2000A, V_{GK} = 15V, R_G = 1Ω V_{AK} = 1000V, L < 20nH, Notes 2 & 3		50		ns
t_{ri}	**Capacitive Discharge, T_J = 125°C**		100		ns
t_d	I_A = 2000A, V_{GK} = 15V, R_G = 1Ω V_{AK} = 1000V, L < 20nH, Notes 2 & 3		50		ns
R_{thJC}				0.18	°C/W
R_{thCS}			0.15		°C/W

TO-247PLUS-HV Outline



PINS:
1 - Gate 2 - Cathode
3, 4 - Anode

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.193	.201	4.90	5.10
A1	.114	.122	2.90	3.10
A2	.075	.083	1.90	2.10
A3	.035	.043	0.90	1.10
b	.053	.059	1.35	1.50
b1	.075	.083	1.90	2.10
c	.022	.030	0.55	0.75
D	.819	.843	20.80	21.40
D1	.638	.646	16.20	16.40
D2	.134	.146	3.40	3.70
D3	.055	.063	1.40	1.60
E	.622	.638	15.80	16.20
E1	.520	.528	13.20	13.40
E2	.118	.126	3.00	3.20
E3	.051	.059	1.30	1.50
e	.100 BSC		2.54 BSC	
e1	.300 BSC		7.62 BSC	
L	.732	.748	18.60	19.00
L1	.106	.118	2.70	3.00
Q	.216	.224	5.50	5.70
R	.165	.169	4.20	4.30

Reverse Diode (FRED)

Symbol	Test Conditions (TJ = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
V_F	I_F = 100A, V_{GK} = 0V, Note 1			2.2	V
I_{RM}	I_F = 50A, V_{GK} = 0V,		29		A
t_{rr}	$-di_F/dt$ = 20A/µs, V_R = 400V		4.1		µs
R_{thJC}				0.36	°C/W

Notes:

1. Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.
2. It is recommended to use a gate driver capable of supplying more than 4Amps and ≥15V gate voltage.
3. Refer to fig. 10 & 11.

PRELIMANARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Extended Output Characteristics @ T_J = 25ºC

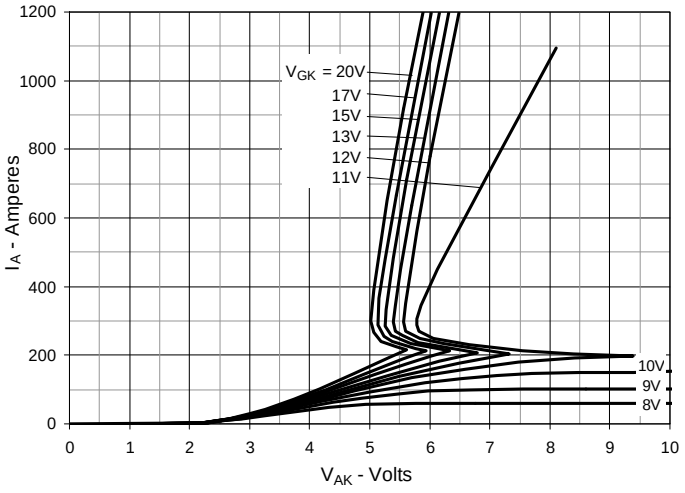


Fig. 2. Extended Output Characteristics @ T_J = 125ºC

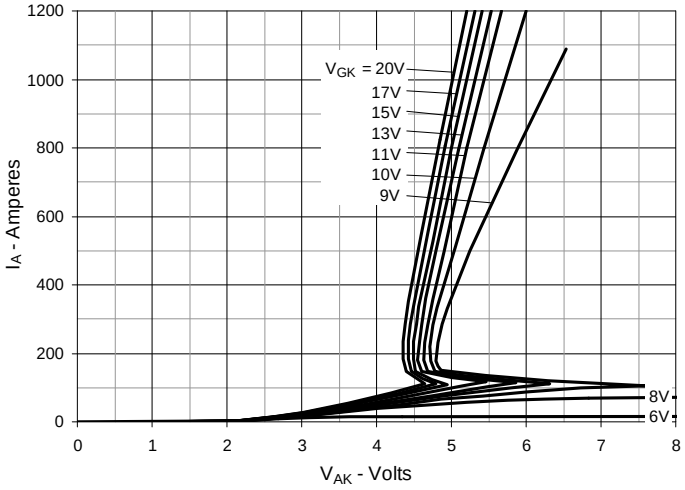


Fig. 3. Extended Output Characteristics @ T_J = - 40ºC

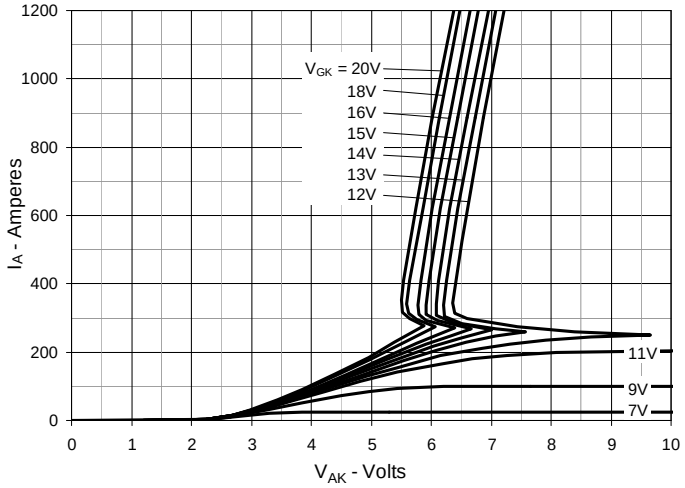


Fig. 4. Gate Charge

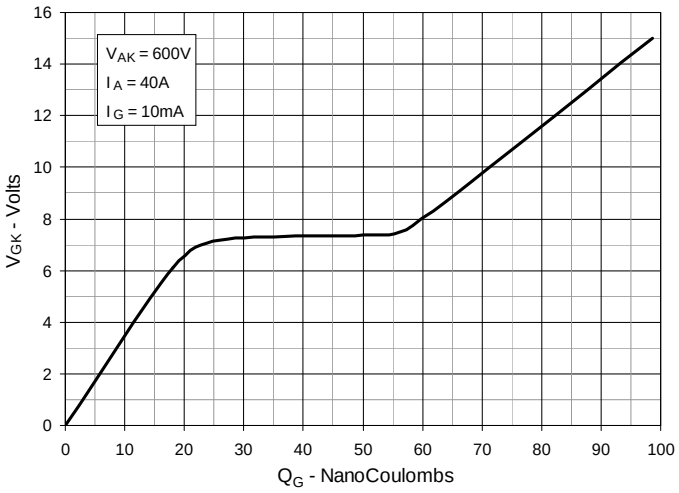


Fig. 5. Capacitance

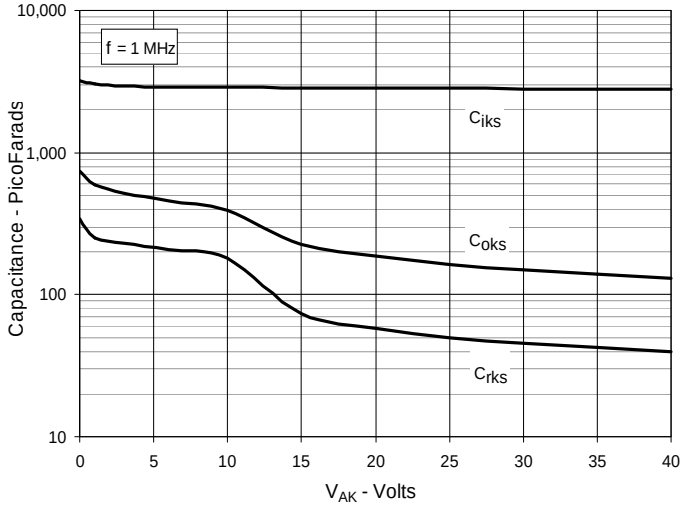
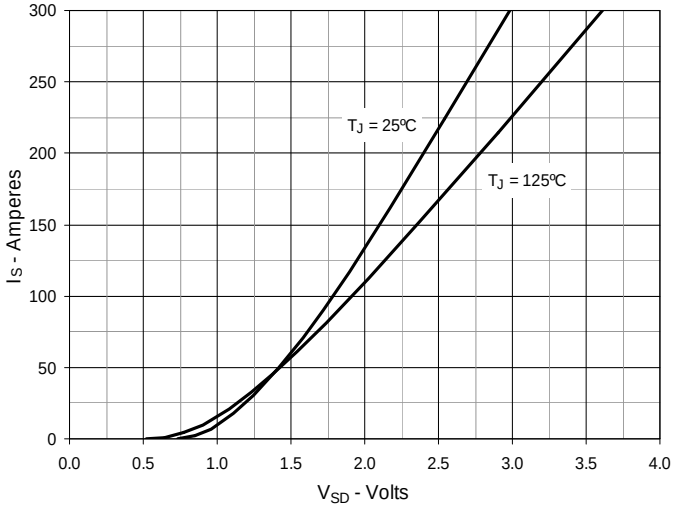


Fig. 6. Forward Voltage Drop of Intrinsic Diode



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Fig. 7. Maximum Transient Thermal Impedance (Thyristor)

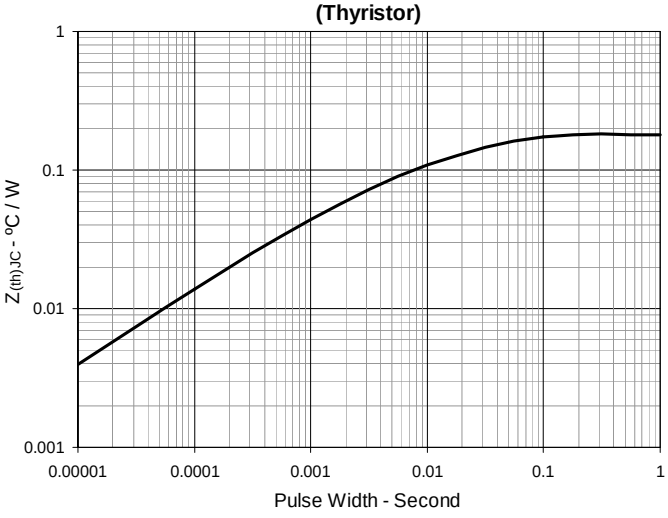


Fig. 8. Maximum Transient Thermal Impedance (Diode)

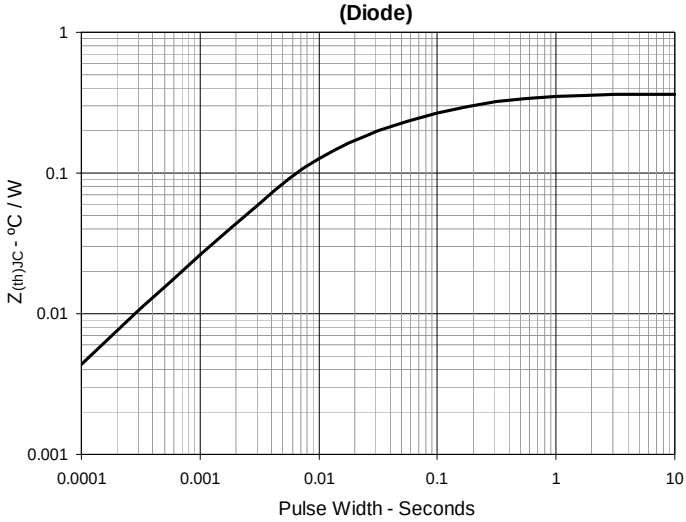
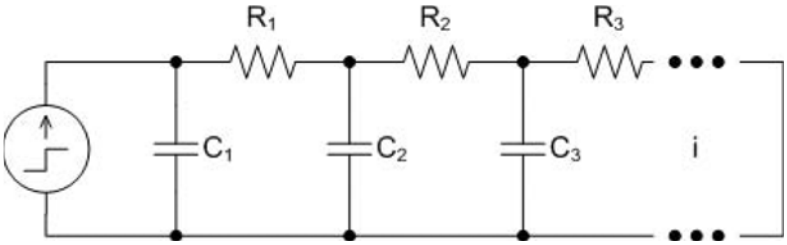


Fig. 9. Cauer Thermal Network



i	Ri (Ω)	Ci (F)
1	0.015004	0.005397
2	0.071079	0.028026
3	0.051007	0.121930
4	0.002310	2.500000

Fig. 10. Capacitive Discharge Circuit

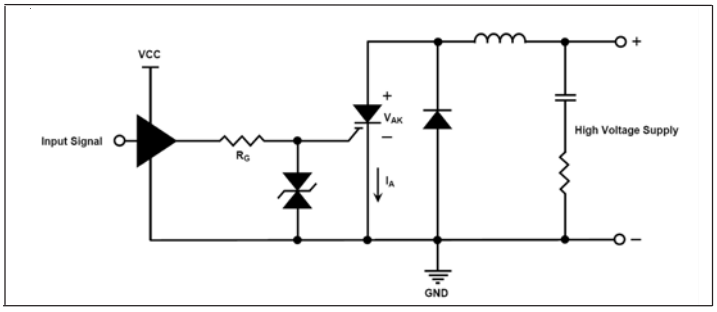
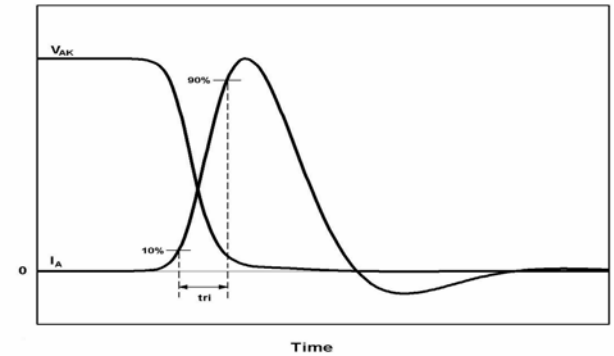


Fig. 11. Capacitive Discharge Waveform



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