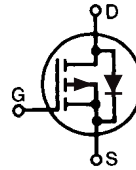


Power MOSFETs

IXTT10P60 IXTH10P60

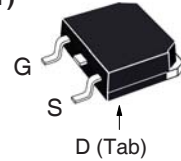
$$\begin{aligned} V_{DSS} &= -600V \\ I_{D25} &= -10A \\ R_{DS(on)} &\leq 1\Omega \end{aligned}$$

P-Channel Enhancement Mode
Avalanche Rated

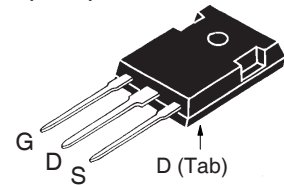


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	- 600	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	- 600	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	- 10	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	- 40	A
I_A	$T_C = 25^\circ\text{C}$	- 10	A
E_{AS}	$T_C = 25^\circ\text{C}$	3	J
P_D	$T_C = 25^\circ\text{C}$	300	W
T_J		- 55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		- 55 ... +150	$^\circ\text{C}$
T_L	1.6mm (0.062in.) from Case for 10s	300	$^\circ\text{C}$
T_{sold}	Plastic Body for 10 seconds	260	$^\circ\text{C}$
M_d	Mounting Torque (TO-247)	1.13 / 10	Nm/lb.in.
Weight	TO-268	4	g
	TO-247	6	g

TO-268 (IXTT)



TO-247 (IXTH)



G = Gate D = Drain
S = Source Tab = Drain

Features

- International Standard Packages
- Low $R_{DS(on)}$ HDMOS™ Process
- Rugged Polysilicon Gate Cell Structure
- Avalanche Rated
- Low Package Inductance
- Easy to Drive and to Protect

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High-Side Switching
- Push Pull Amplifiers
- DC Choppers
- Automatic Test Equipment

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = -250\mu A$	- 600		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	- 3.0		- 5.0 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			- 25 μA - 1 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			1 Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = -10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	5	10.5	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = -25\text{V}$, $f = 1\text{MHz}$		4665	pF
C_{oss}			437	pF
C_{rss}			157	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 4.7\Omega$ (External)		33	ns
t_r			27	ns
$t_{d(off)}$			85	ns
t_f			35	ns
$Q_{g(on)}$	$V_{GS} = -10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		135	nC
Q_{gs}			30	nC
Q_{gd}			45	nC
R_{thJC}	TO-247			0.42 $^\circ\text{C/W}$
R_{thCS}		0.21		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			- 10 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			- 40 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			- 3.0 V
t_{rr}	$I_F = -10\text{A}$, $-di/dt = -100\text{A}/\mu\text{s}$ $V_R = -100\text{V}$, $V_{GS} = 0\text{V}$		500	ns

Note 1: Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

TO-247 Outline

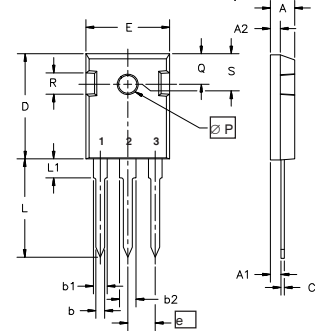


Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

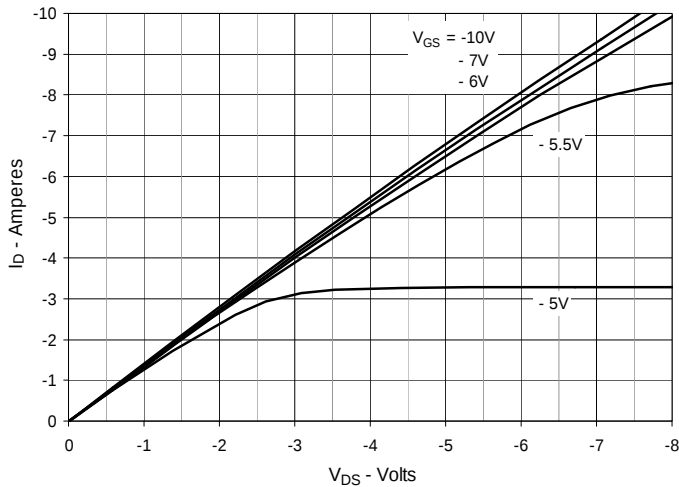


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

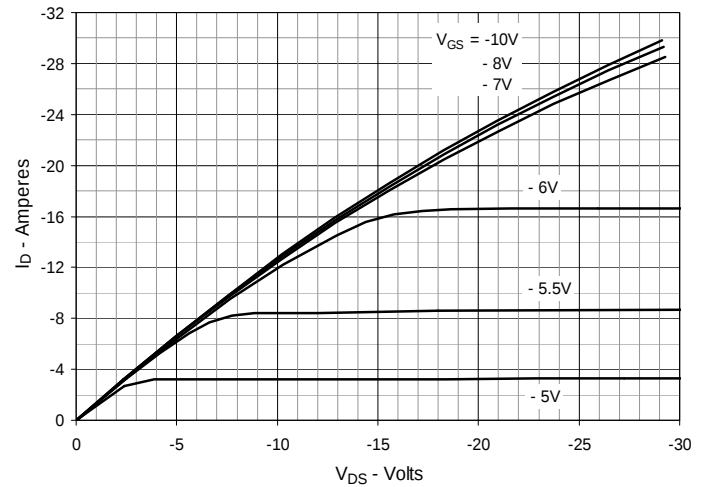


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

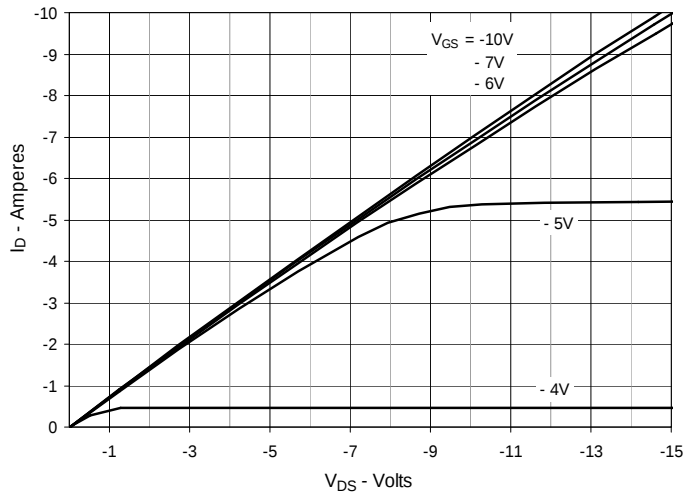


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = -5\text{A}$ Value vs. Junction Temperature

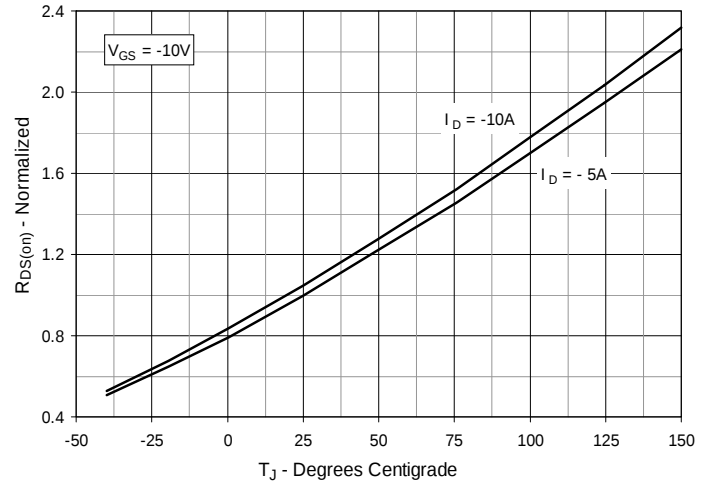


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = -5\text{A}$ Value vs. Drain Current

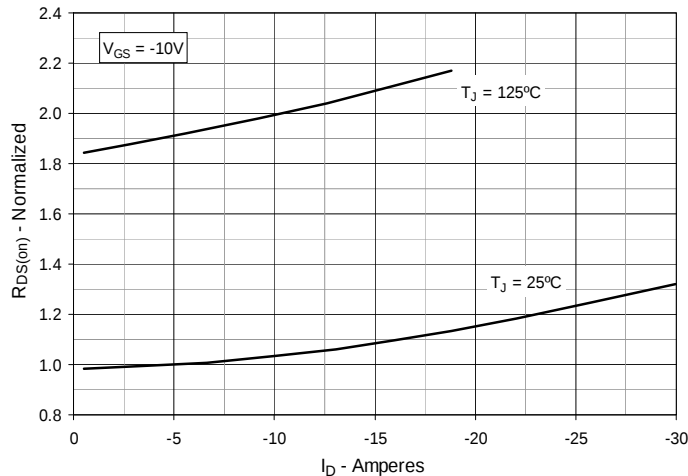


Fig. 6. Maximum Drain Current vs. Case Temperature

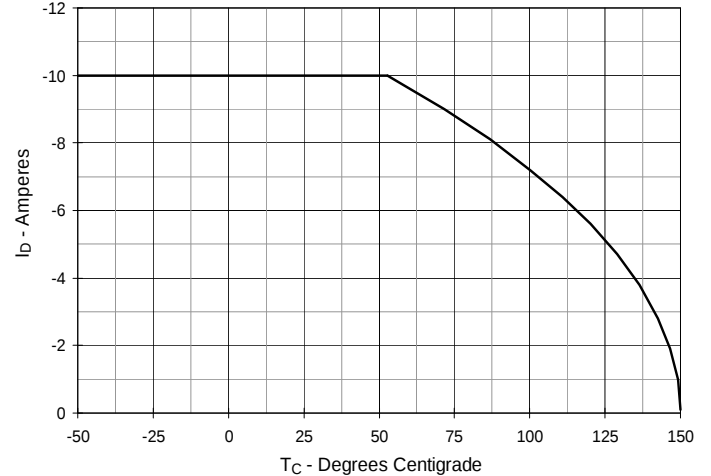


Fig. 7. Input Admittance

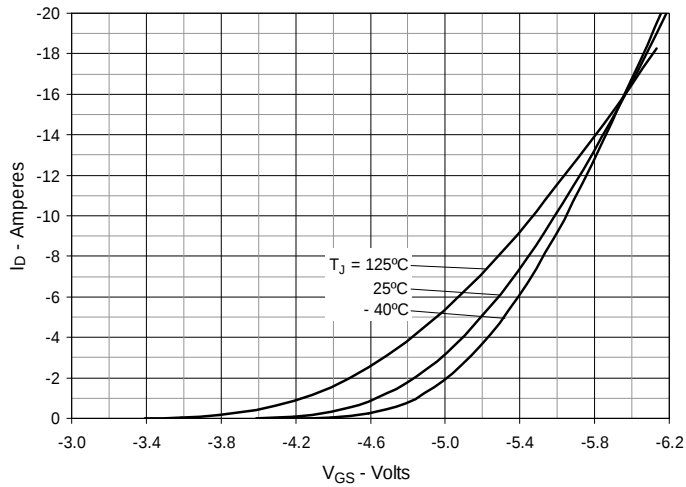


Fig. 8. Transconductance

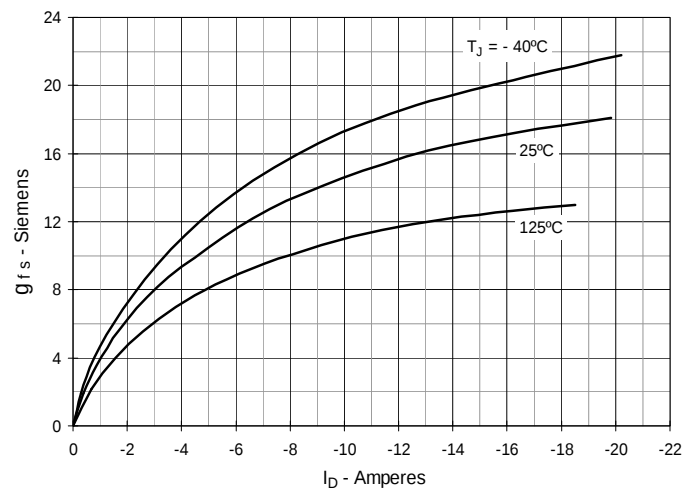


Fig. 9. Forward Voltage Drop of Intrinsic Diode

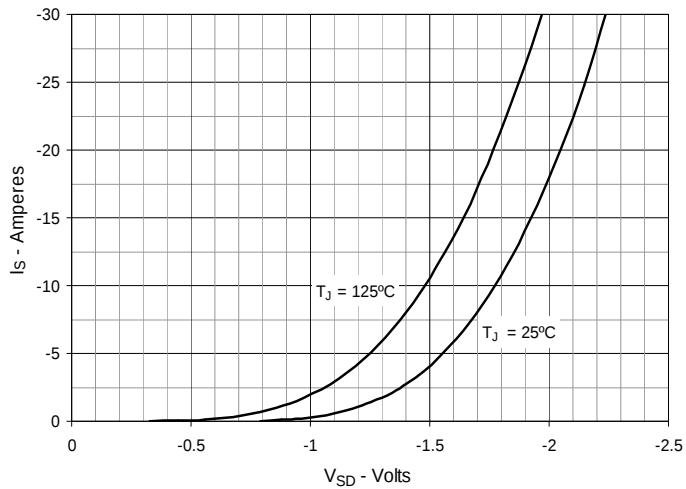


Fig. 10. Gate Charge

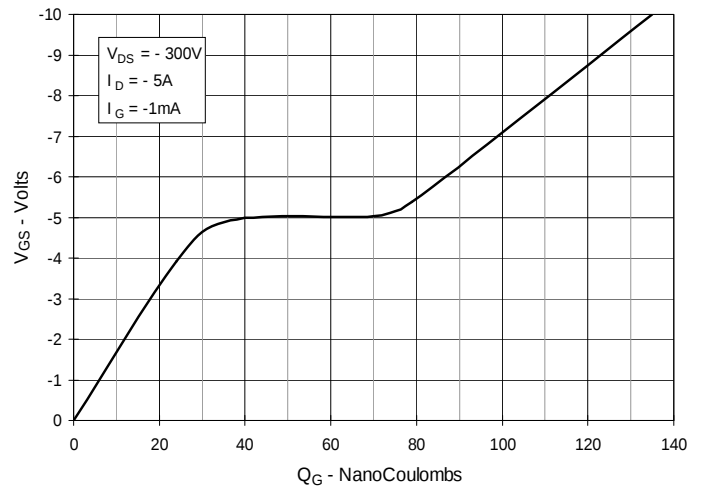


Fig. 11. Capacitance

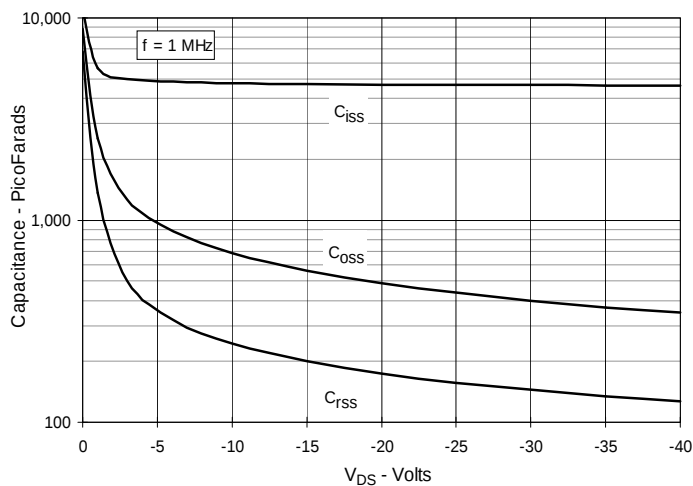


Fig. 12. Maximum Transient Thermal Impedance

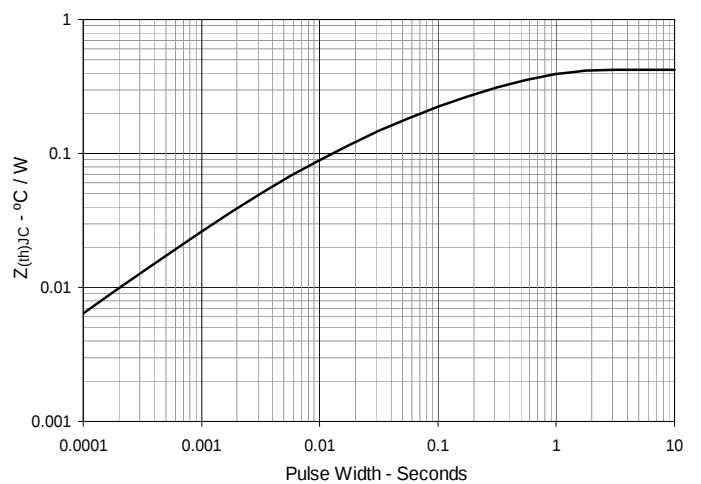


Fig. 13. Forward-Bias Safe Operating Area

@ $T_C = 25^\circ\text{C}$

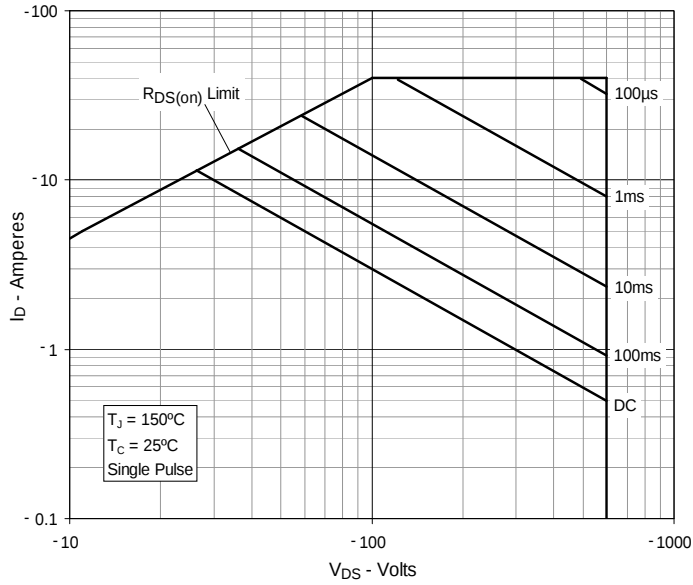
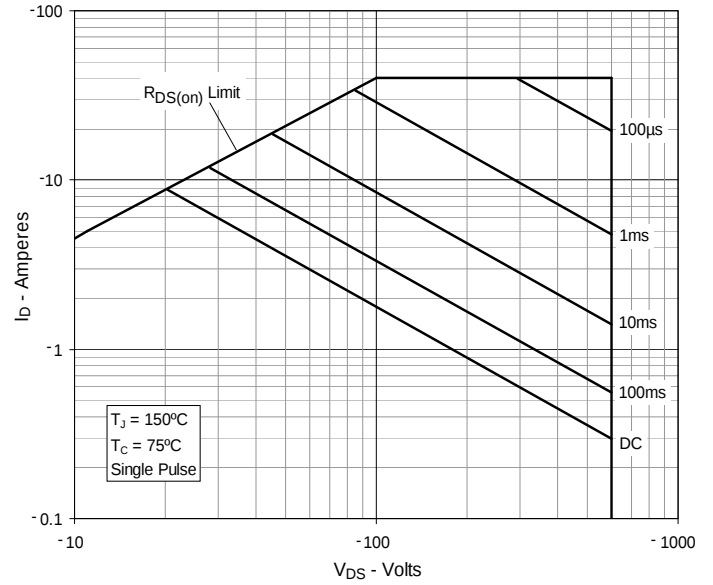


Fig. 14. Forward-Bias Safe Operating Area

@ $T_C = 75^\circ\text{C}$





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