IXYS

Preliminary Technical Information

GenX3™ 600V IGBTs

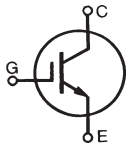
(Electrically Isolated Back Surface)

Medium-Speed Low-Vsat PT IGBTs 5-40 kHz Switching

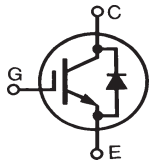
IXGR48N60B3*
IXGR48N60B3D1

*ObsoletePartNumber

V_{CES} = 600V
I_{C25} = 60A
$V_{CE(sat)}$ ≤ 2.1V
$t_{fi(typ)}$ = 116ns

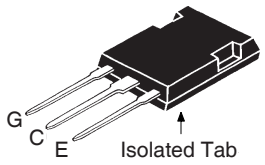


IXGR_B3



IXGR_B3D1

ISOPLUS247™
E153432



G = Gate E = Emitter
C = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	600	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	600	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	60	A
I_{C110}	T_C = 110°C	27	A
I_{F110}	T_C = 110°C (48N60B3D1)	27	A
I_{CM}	T_C = 25°C, 1ms	280	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 5Ω Clamped Inductive Load	I_{CM} = 120 @ ≤ V_{CE}	A
P_C	T_C = 25°C	150	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10 seconds	260	°C
F_C	Mounting Force	20..120 / 4.5..27	N/lb.
V_{ISOL}	50/60 Hz, RM, t = 1min	2500	V~
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)		Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V		600			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}		3.0		5.5	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V	48N60B3			25	μA
		48N60B3D1			1.75	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 20V				±100	nA
$V_{CE(sat)}$	I_C = 40A, V_{GE} = 15V, Note 1			1.77	2.1	V
		T_J = 125°C		1.74		V

Features

- Silocon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- Optimized for Low Conduction and Switching Losses
- 2500V~ Electrical Isolation
- Anti-Parallel Ultra Fast Diode
- Square RBSOA

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts

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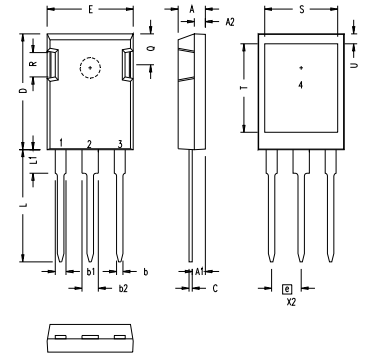
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)		Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 30A, V_{CE} = 10V, Note 1		20	30		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz			2980		pF
C_{oes}		48N60B3		170		pF
		48N60B3D1		200		pF
C_{res}				45		pF
Q_g	I_C = 40A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}			115		nC
Q_{ge}				21		nC
Q_{gc}				40		nC
$t_{d(on)}$	**Inductive Load, T_J = 25°C**			22		ns
t_{ri}	I_C = 30A, V_{GE} = 15V			25		ns
E_{on}	V_{CE} = 480V, R_G = 5Ω			0.84		mJ
$t_{d(off)}$	Note 2			130	200	ns
t_{fi}				116	200	ns
E_{off}				0.66	1.20	mJ
$t_{d(on)}$	**Inductive Load, T_J = 125°C**			19		ns
t_{ri}	I_C = 30A, V_{GE} = 15V			25		ns
E_{on}	V_{CE} = 480V, R_G = 5Ω			1.71		mJ
$t_{d(off)}$	Note 2			190		ns
t_{fi}				157		ns
E_{off}				1.30		mJ
R_{thJC}					0.83	°C/W
R_{thCS}				0.15		°C/W

ISOPLUS247 (IXGR) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Reverse Diode (FRED) (D1 Version ONLY)

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)		Characteristic Values Min.	Typ.	Max.	
V_F	I_F = 30A, V_{GE} = 0V, Note 1				2.8	V
		T_J = 150°C		1.6		V
I_{RM}	I_F = 30A, V_{GE} = 0V, V_R = 100V			4		A
	$-di_F/dt$ = 100A/μs					
t_{rr}	I_F = 1A, -di/dt = 100A/μs, V_R = 30V	T_J = 100°C		100		ns
R_{thJC}					1.5	°C/W
R_{thCS}				1.5		°C/W

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Switching times & energy losses may increase for higher V_{CE}(clamp), T_J or R_G.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

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