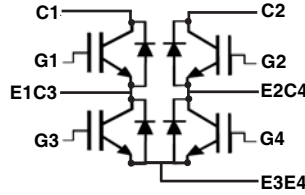


High Voltage, High Gain BIMOSFET™ Monolithic Bipolar MOS Transistor

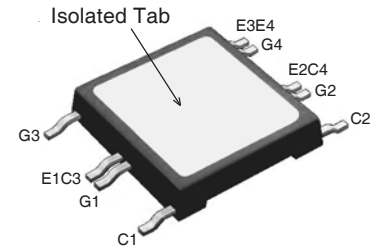
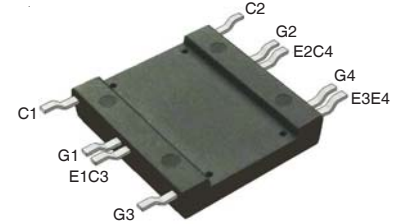
MMIX4B22N300

(Electrically Isolated Tab)



$$\begin{aligned} V_{CES} &= 3000V \\ I_{C90} &= 22A \\ V_{CE(sat)} &\leq 2.7V \end{aligned}$$

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	3000	V
V_{CGR}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}, R_{GE} = 1M\Omega$	3000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ\text{C}$	38	A
I_{C90}	$T_C = 90^\circ\text{C}$	22	A
I_{CM}	$T_C = 25^\circ\text{C}, 1\text{ms}$	165	A
SSOA (RBSOA)	$V_{GE} = 15V, T_{VJ} = 125^\circ\text{C}, R_G = 15\Omega$ Clamped Inductive Load	$I_{CM} = 180$ $V_{CES} \leq 1500$	A V
T_{SC} (SCSOA)	$V_{GE} = 15V, T_J = 125^\circ\text{C},$ $R_G = 52\Omega, V_{CE} = 1500V, \text{Non-Repertitive}$	10	μs
P_C	$T_C = 25^\circ\text{C}$	150	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	Plastic Body for 10s	260	$^\circ\text{C}$
F_C	Mounting Force	50..200 / 11..45	N/lb
V_{ISOL}	50/60Hz, 1 minute	4000	V~
Weight		8	g



G = Gate
C = Collector

E = Emitter

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Capacitor Discharge Circuits

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu\text{A}, V_{GE} = 0V$	3000		V
$V_{GE(th)}$	$I_C = 250\mu\text{A}, V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = V_{CES}, V_{GE} = 0V$ Note 2, $T_J = 125^\circ\text{C}$			35 μA 1.5 mA
I_{GES}	$V_{CE} = 0V, V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 22A, V_{GE} = 15V, \text{Note 1}$ $T_J = 125^\circ\text{C}$		2.2 2.7	V V

Symbol Test Conditions(T_J = 25°C Unless Otherwise Specified)**Characteristic Values****Min. Typ. Max.**

g_{fs}	I _C = 22A, V _{CE} = 10V, Note 1	13	22	S
C_{ies}	V _{CE} = 25V, V _{GE} = 0V, f = 1MHz		2200	pF
C_{oes}			85	pF
C_{res}			30	pF
Q_{g(on)}	I _C = 22A, V _{GE} = 15V, V _{CE} = 1500V		110	nC
Q_{ge}			13	nC
Q_{gc}			45	nC
t_{d(on)}	Resistive Switching Times, T_J = 25°C I _C = 22A, V _{GE} = 15V V _{CE} = 960V, R _G = 15Ω		46	ns
t_r			360	ns
t_{d(off)}			205	ns
t_f			1820	ns
t_{d(on)}	Resistive Switching Times, T_J = 125°C I _C = 22A, V _{GE} = 15V V _{CE} = 960V, R _G = 15Ω		43	ns
t_r			700	ns
t_{d(off)}			220	ns
t_f			1650	ns
R_{thJC}			0.05	0.83 °C/W
R_{thCS}				°C/W
R_{thJA}			30	°C/W

Reverse Diode**Symbol Test Conditions**(T_J = 25°C Unless Otherwise Specified)**Characteristic Values****Min. Typ. Max**

V_F	I _F = 22A, V _{GE} = 0V, Note 1		2.7	V
t_{rr}	I _F = 11A, V _{GE} = 0V, -di _F /dt = 100A/μs V _R = 100V, V _{GE} = 0V		1.4	μs
I_{RM}			30	A
Q_{RM}			21	μC

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Device must be heatsunk for high temperature leakage current measurements to avoid thermal runaway.

Additional provisions for lead-to-lead voltage isolation are required at V_{CE} > 1200V.

IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

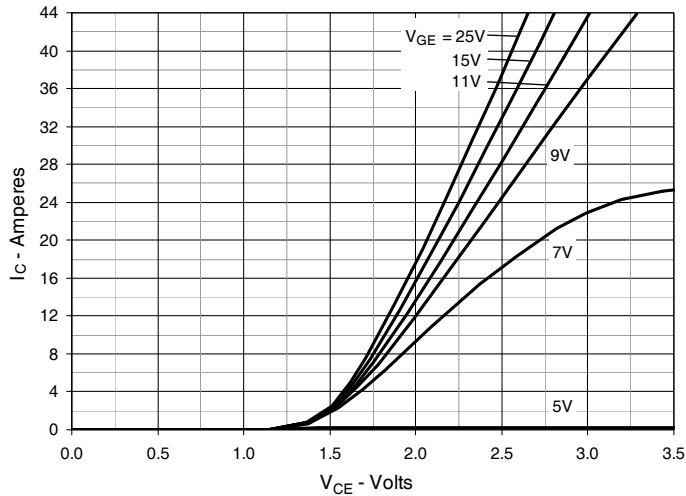
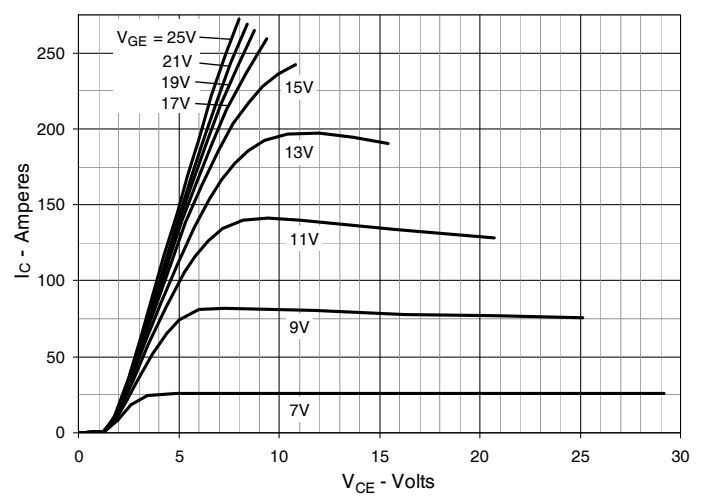
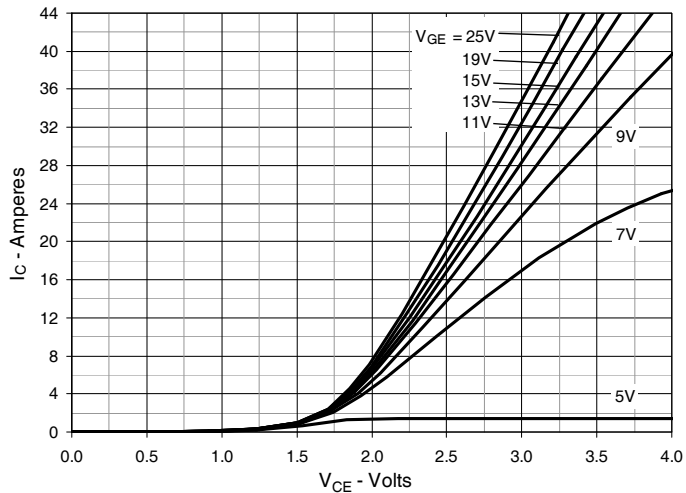
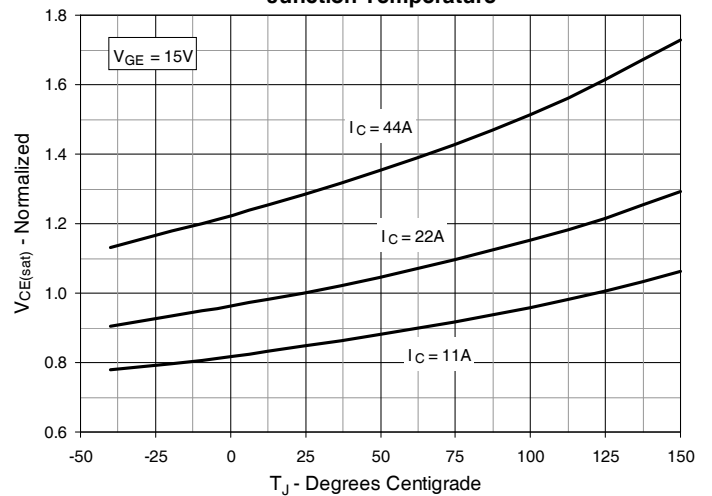
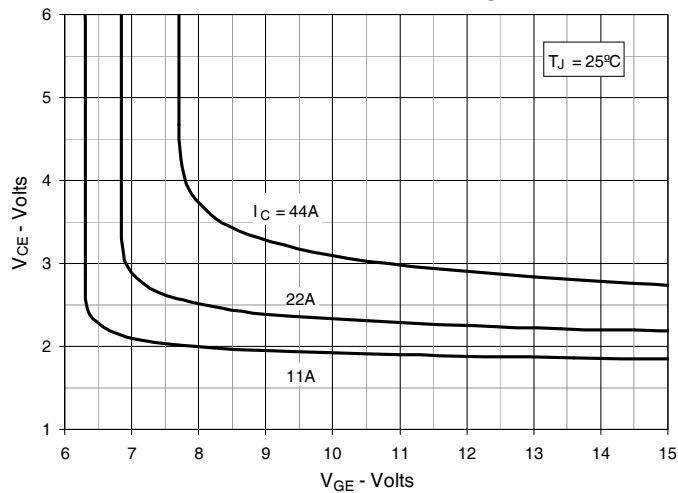
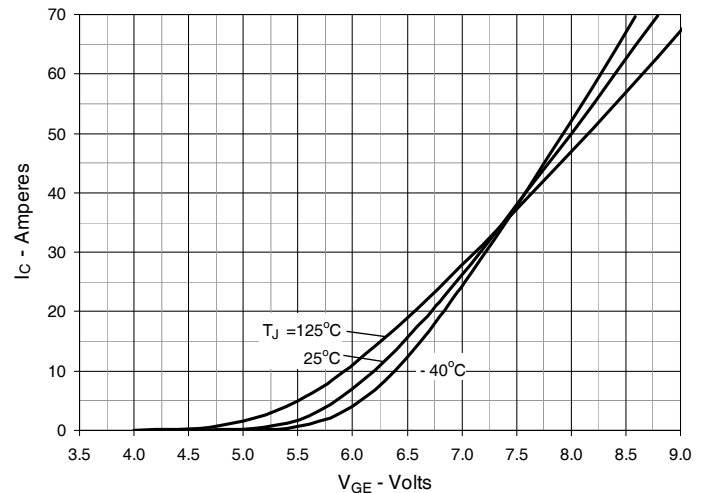
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

Fig. 6. Input Admittance


Fig. 7. Transconductance

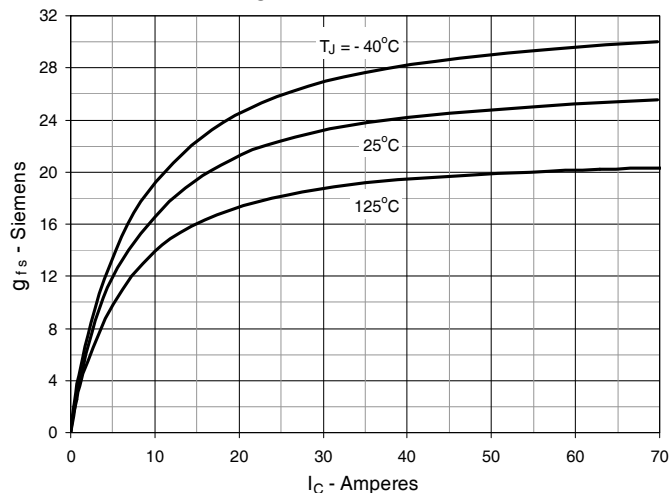


Fig. 8. Gate Charge

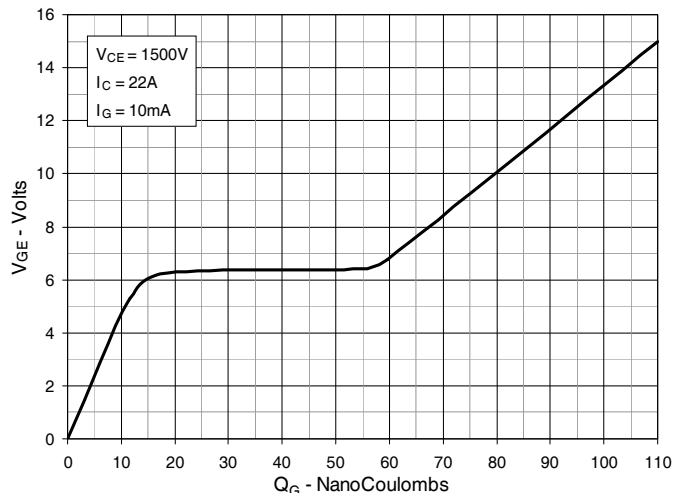


Fig. 9. Forward Voltage Drop of Intrinsic Diode

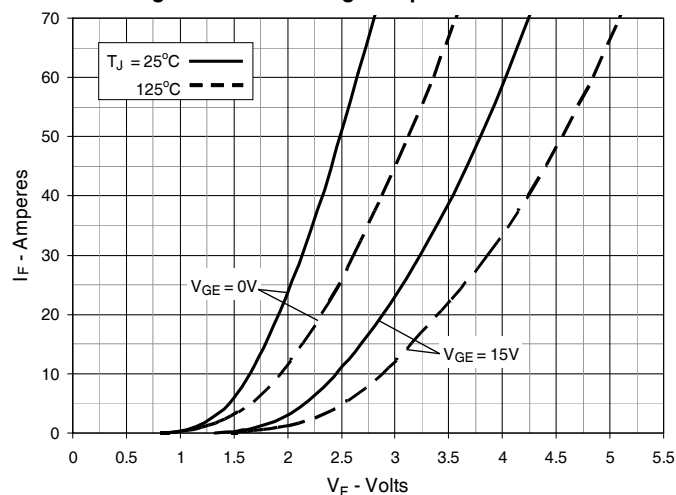


Fig. 10. Capacitance

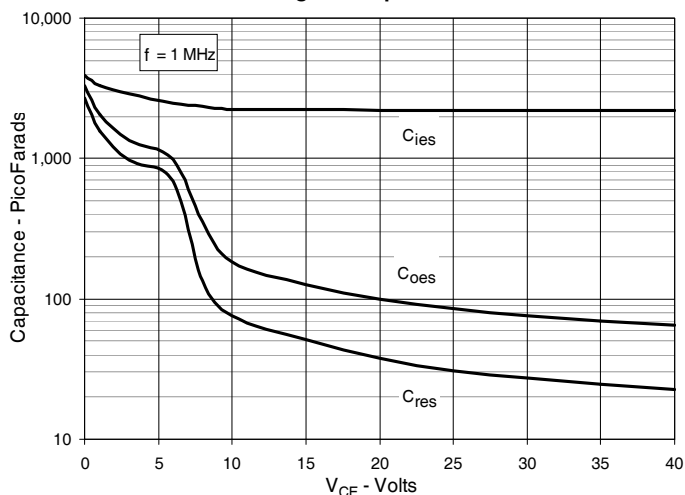


Fig. 11. Reverse-Bias Safe Operating Area

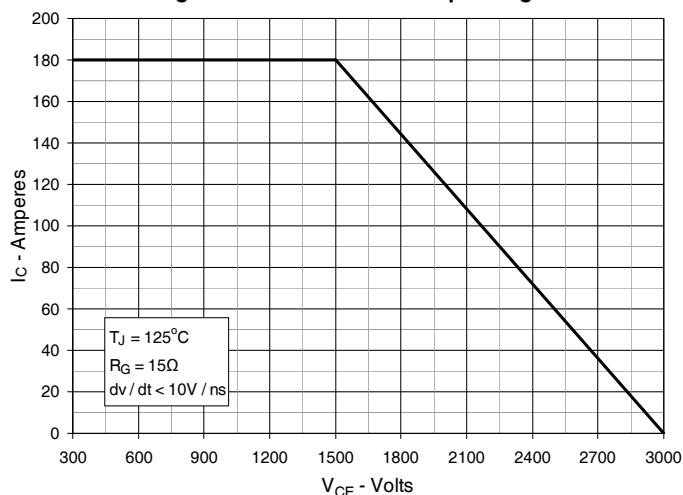


Fig. 12. Maximum Transient Thermal Impedance

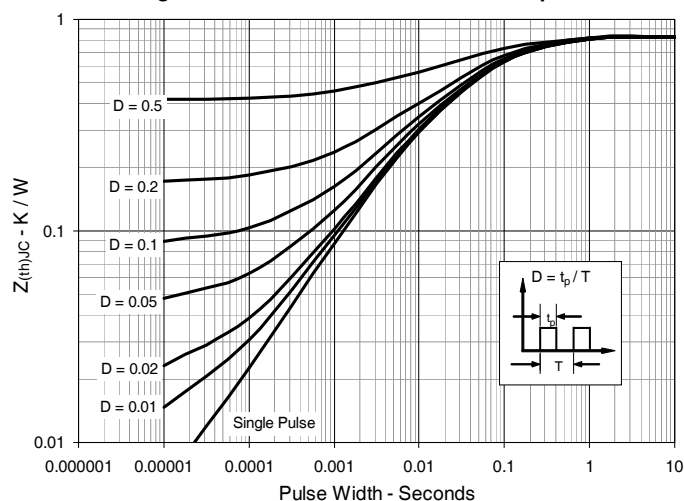


Fig. 13. Forward-Bias Safe Operating Area @ $T_C = 25^\circ\text{C}$

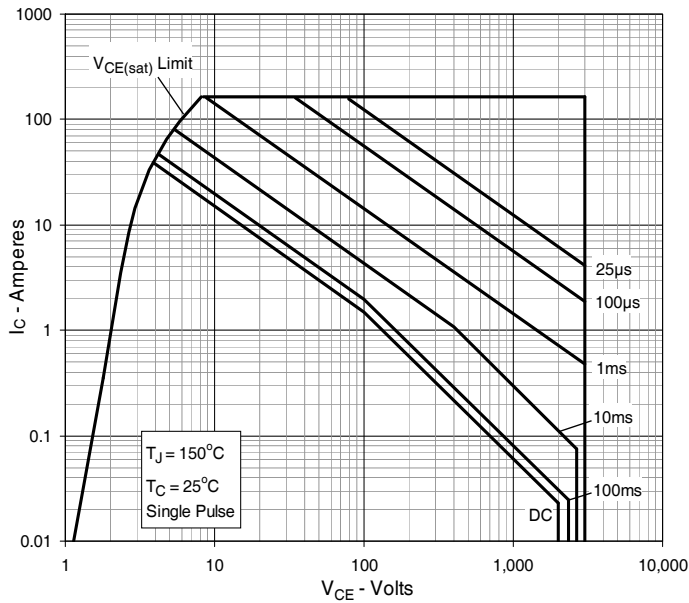
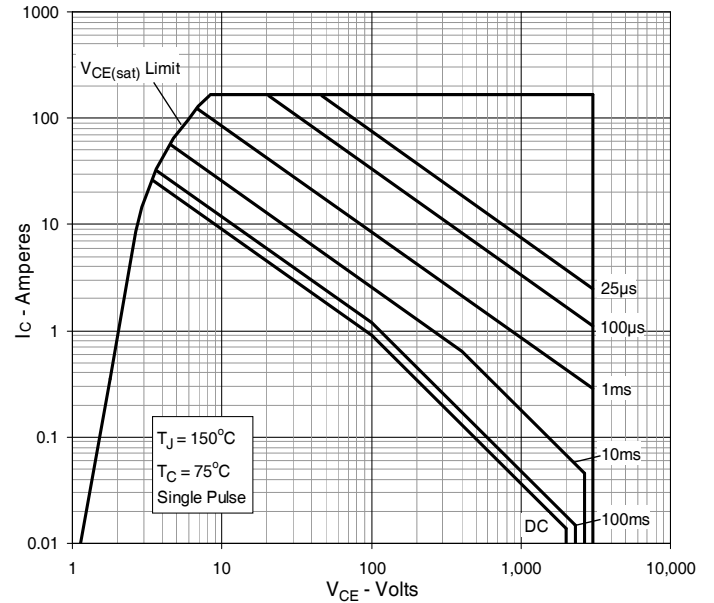
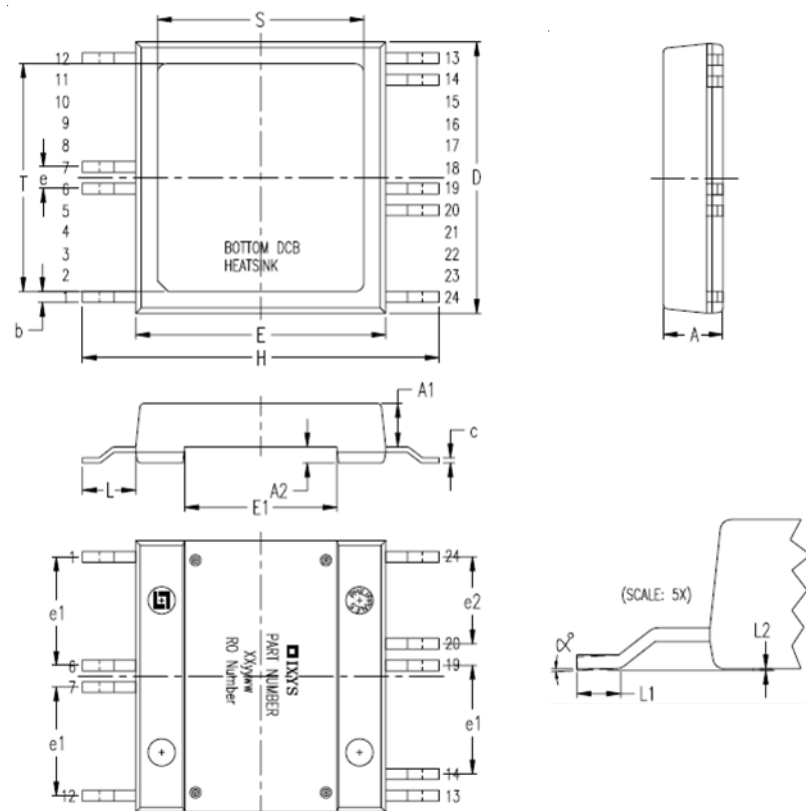


Fig. 14. Forward-Bias Safe Operating Area @ $T_C = 75^\circ\text{C}$



Package Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.394 BSC		10.00 BSC	
e2	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
α	0	4°	0	4°