

HiPerFET™

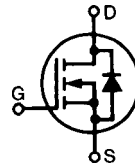
Power MOSFETs

N-Channel Enhancement Mode
High dv/dt, Low t_{rr} , HDMOS™ Family

IXFH 76 N06-11
IXFH 76 N06-12
IXFH 76 N07-11
IXFH 76 N07-12

V_{DSS}	I_{D25}	$R_{DS(on)}$
60 V	76 A	11 mΩ
60 V	76 A	12 mΩ
70 V	76 A	11 mΩ
70 V	76 A	12 mΩ

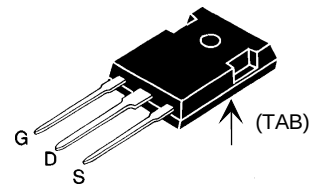
Preliminary data sheet



Symbol	Test Conditions	Maximum Ratings		
V_{DSS}	$T_J = 25^\circ\text{C}$ to 175°C	N06	60	V
		N07	70	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 10\text{ k}\Omega$	N06	60	V
		N07	70	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	$T_C = 25^\circ\text{C}$ (Chip capability = 125 A)		76	A
I_{D119}	$T_C = 119^\circ\text{C}$, limited by external leads		76	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}		304	A
I_{AR}	$T_C = 25^\circ\text{C}$		100	A
E_{AR}	$T_C = 25^\circ\text{C}$		30	mJ
E_{AS}			2	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 2\ \Omega$		5	V/ns
P_D	$T_C = 25^\circ\text{C}$		360	W
T_J			-55 ... +175	°C
T_{JM}			175	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s		300	°C
M_d	Mounting torque		1.15/10	Nm/lb.in.
Weight			6	g

Symbol	Test Conditions	Characteristic Values (T _J = 25°C, unless otherwise specified)		
		min.	typ.	max.
V _{DSS}	V _{GS} = 0 V, I _D = 250 μA	N06	60	V
		N07	70	V
V _{GS(th)}	V _{DS} = V _{GS} , I _D = 4 mA		2.0	3.4 V
I _{GSS}	V _{GS} = ±20 V _{DC} , V _{DS} = 0			±100 nA
I _{DSS}	V _{DS} = 0.8 • V _{DSS}	T _J = 25°C		100 μA
	V _{GS} = 0 V	T _J = 125°C		500 μA
R _{DS(on)}	V _{GS} = 10 V, I _D = 40 A	76N06/N07-11		11 mΩ
		76N06/N07-12		12 mΩ
	Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			

TO-247 AD



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard package JEDEC TO-247 AD
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
 - easy to drive and to protect
- Fast intrinsic Rectifier

Applications

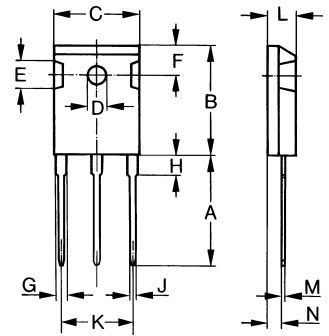
- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls
- Low voltage relays

Advantages

- Easy to mount with 1 screw (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	$V_{DS} = 10\text{ V}; I_D = 40\text{ A}$, pulse test	30	40	S
C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		4400	pF
C_{oss}			2000	pF
C_{rss}			1200	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 30\text{ A}$ $R_G = 1\ \Omega$ (External)		40	ns
t_r			70	ns
$t_{d(off)}$			130	ns
t_f			55	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 40\text{ A}$		240	nC
Q_{gs}			30	nC
Q_{gd}			120	nC
R_{thJC}			0.42	K/W
R_{thCK}		0.25		K/W

Source-Drain Diode		Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
Symbol	Test Conditions	min.	typ.	max.
I_S	$V_{GS} = 0\text{ V}$			76 A
I_{SM}	Repetitive; pulse width limited by T_{JM}			304 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			1.5 V
t_{rr}	$I_F = 25\text{ A}, -di/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$ $V_R = 25\text{ V}, T_J = 125^\circ\text{C}$		150	ns 250 ns

TO-247 AD (IXFH) Outline


Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	19.81	20.32	0.780	0.800
B	20.80	21.46	0.819	0.845
C	15.75	16.26	0.610	0.640
D	3.55	3.65	0.140	0.144
E	4.32	5.49	0.170	0.216
F	5.4	6.2	0.212	0.244
G	1.65	2.13	0.065	0.084
H	-	4.5	-	0.177
J	1.0	1.4	0.040	0.055
K	10.8	11.0	0.426	0.433
L	4.7	5.3	0.185	0.209
M	0.4	0.8	0.016	0.031
N	1.5	2.49	0.087	0.102

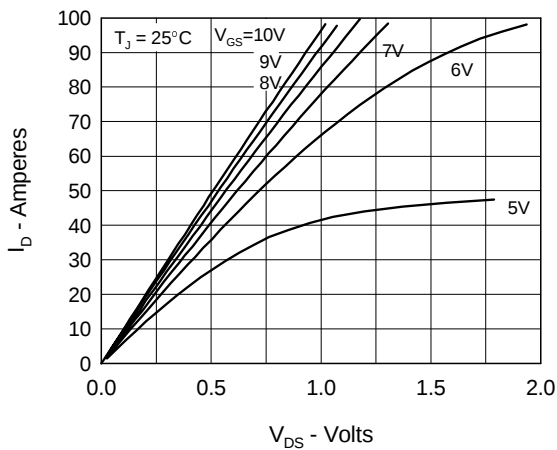
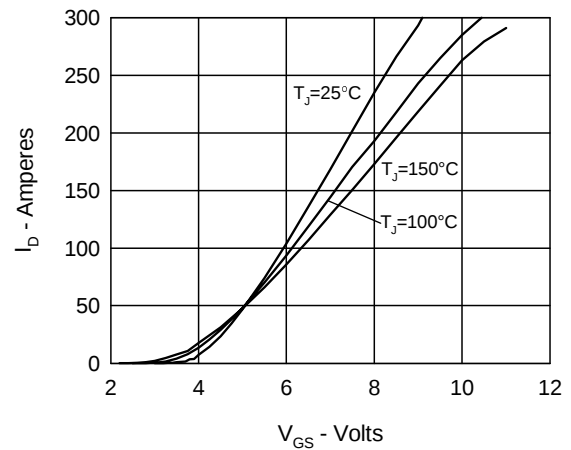
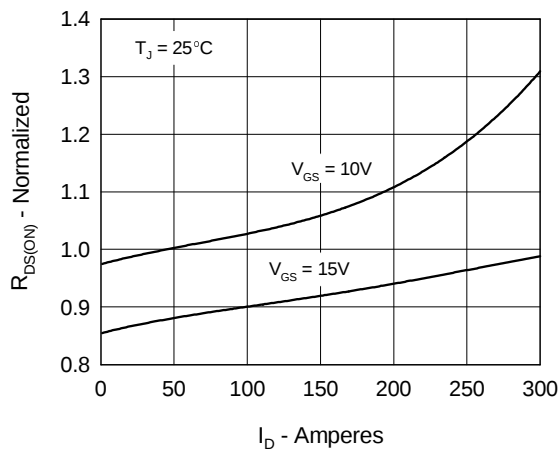
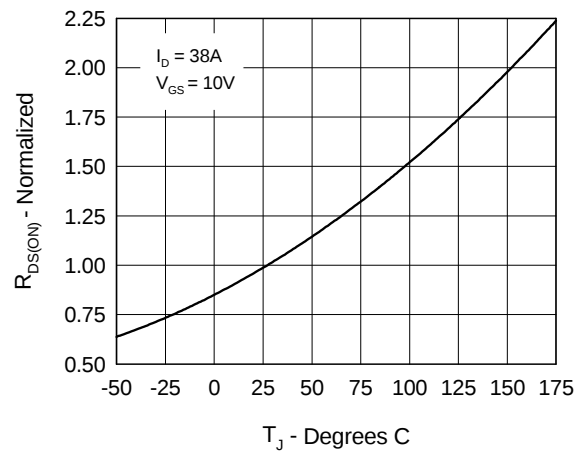
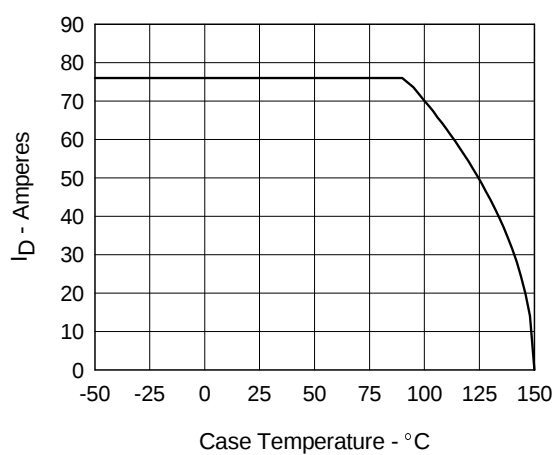
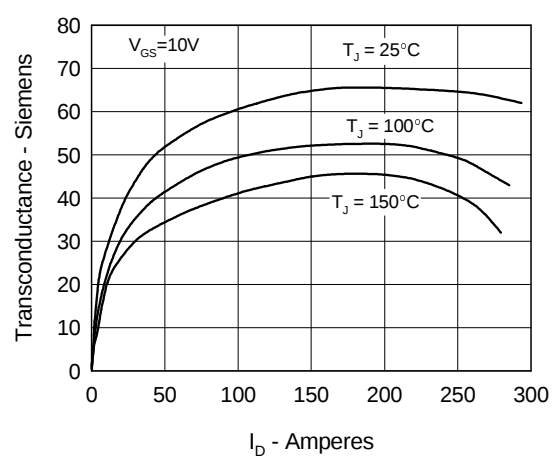
Fig.1 Output Characteristics

Fig. 2 Input Admittance

Fig. 3 $R_{DS(on)}$ vs. Drain Current

Fig. 4 $R_{DS(on)}$ Temperature Dependence

Fig. 5 I_D vs. Case Temperature

Fig. 6 Transconductance


Fig. 7 Gate Charge

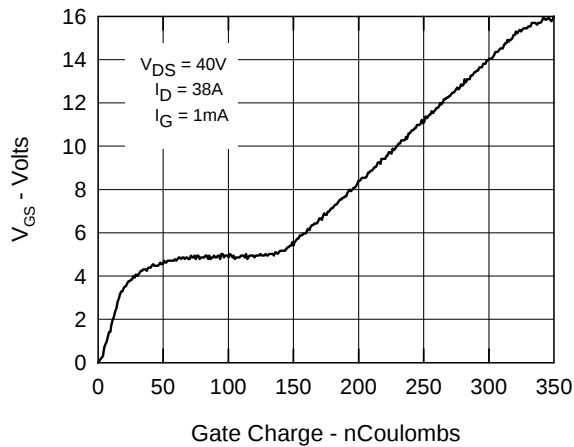


Fig. 8 Forward Bias Safe Operating Area

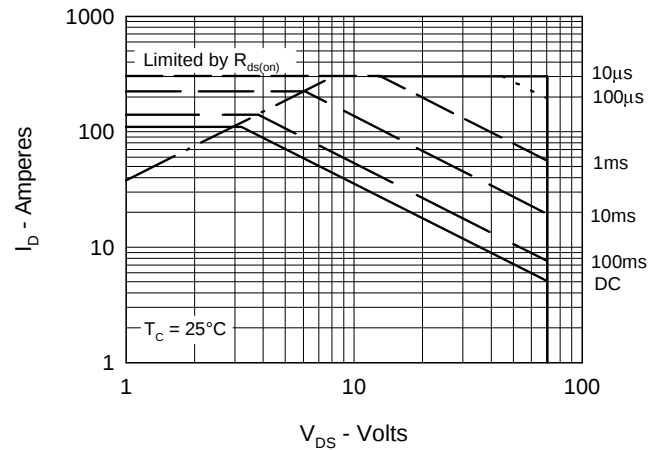


Fig. 9 Capacitance Curves

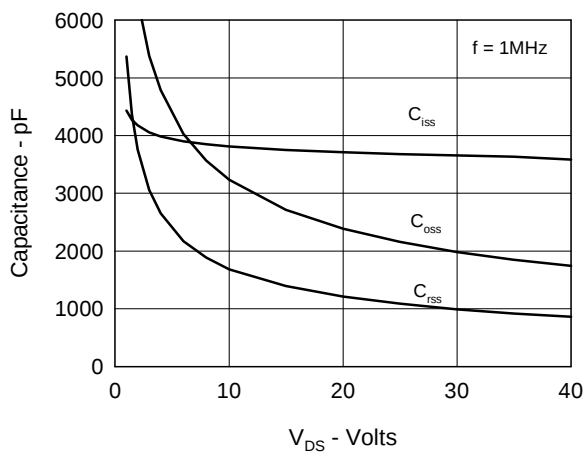


Fig. 10 Source Current vs. Source to Drain Voltage

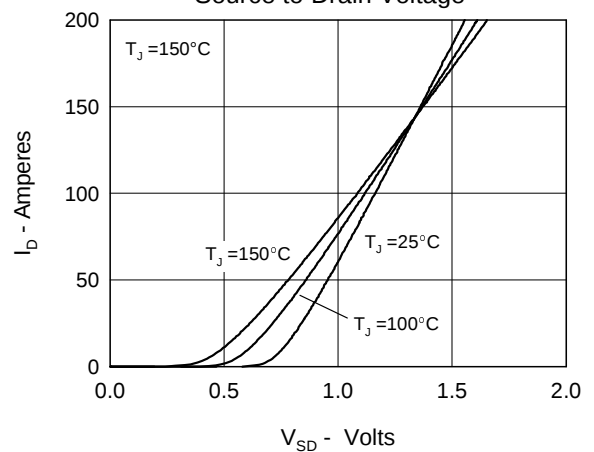
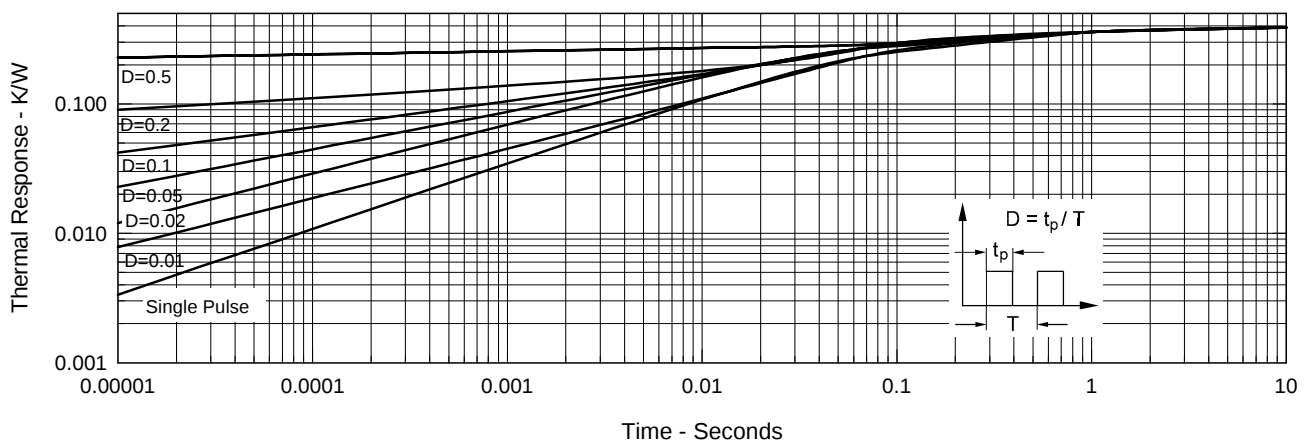


Fig. 11 Transient Thermal Impedance





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