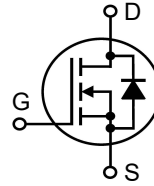


X3-Class HiPerFET™ Power MOSFET

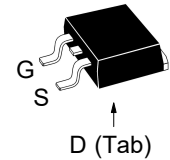
IXFA36N60X3

$$\begin{aligned} V_{DSS} &= 600V \\ I_{D25} &= 36A \\ R_{DS(on)} &\leq 90m\Omega \end{aligned}$$

N-Channel Enhancement Mode
Avalanche Rated



TO-263
(IXFA)



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	600	V
V_{DGR}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}, R_{GS} = 1M\Omega$	600	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	36	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	48	A
I_A	$T_C = 25^\circ\text{C}$	8	A
E_{AS}	$T_C = 25^\circ\text{C}$	750	mJ
dv/dt	$I_S \leq I_{DM}, V_{DD} \leq V_{DSS}, T_J \leq 150^\circ\text{C}$	50	V/ns
P_D	$T_C = 25^\circ\text{C}$	446	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_{SOLD}	Plastic Body for 10s	260	$^\circ\text{C}$
F_C	Mounting Force	10..65 / 2.2..14.6	N/lb
Weight		2.5	g

G = Gate D = Drain
S = Source Tab = Drain

Features

- International Standard Package
- Low $R_{DS(ON)}$ and Q_G
- Avalanche Rated
- Low Package Inductance

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V, I_D = 1mA$	600		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 2.5mA$	3.5		5.0 V
I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			25 μA 1 mA
$R_{DS(on)}$	$V_{GS} = 10V, I_D = 0.5 \cdot I_{D25}$, Note 1			90 m Ω

Symbol	Test Conditions ($T_J = 25^{\circ}\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	16	26	S
R_{Gi}	Gate Input Resistance		2.1	Ω
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		2030	pF
C_{oss}			3050	pF
C_{rss}			3.6	pF
Effective Output Capacitance				
$C_{o(er)}$	Energy related	$V_{GS} = 0\text{V}$ $V_{DS} = 0.8 \cdot V_{DSS}$	110	pF
$C_{o(tr)}$	Time related		510	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 10\Omega$ (External)		23	ns
t_r			8	ns
$t_{d(off)}$			45	ns
t_f			4	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		29	nC
Q_{gs}			10	nC
Q_{gd}			10	nC
R_{thJC}				0.28 $^{\circ}\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max
I_S	$V_{GS} = 0\text{V}$			36 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			144 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.4 V
t_{rr}	$I_F = 18\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$		180	ns
Q_{RM}			1.6	μC
I_{RM}			18.0	A

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

Littelfuse reserves the right to change limits, test conditions and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065B1	6,683,344	6,727,585	7,005,734B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123B1	6,534,343	6,710,405B2	6,759,692	7,063,975B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728B1	6,583,505	6,710,463	6,771,478B2	7,071,537	

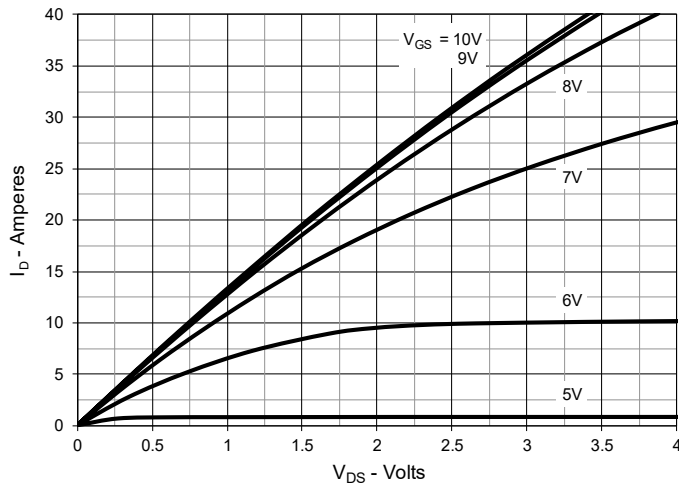
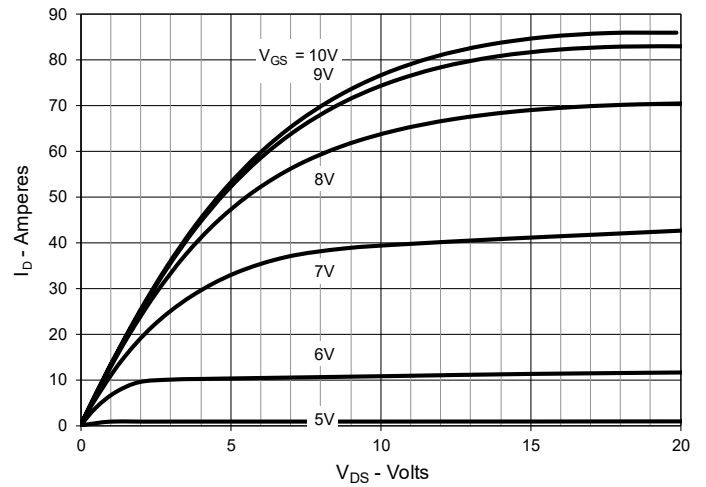
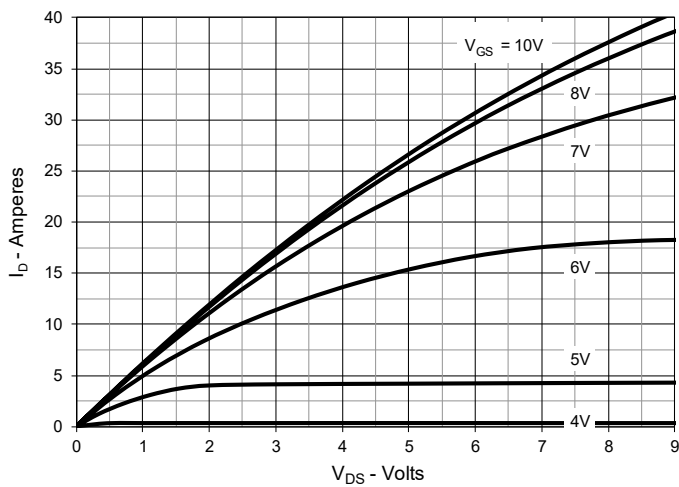
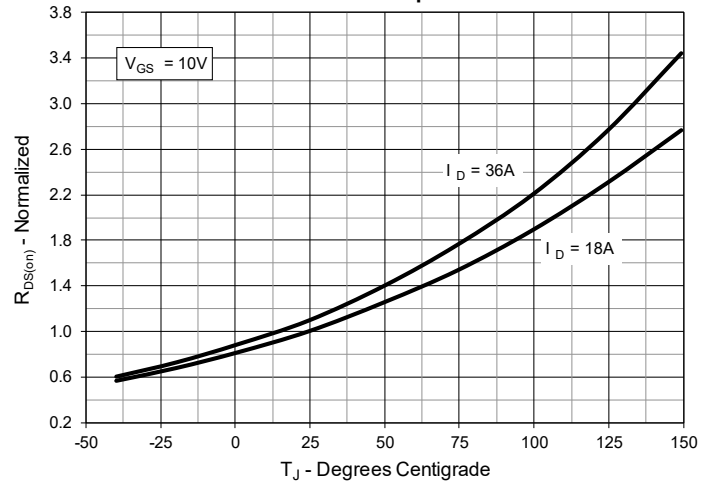
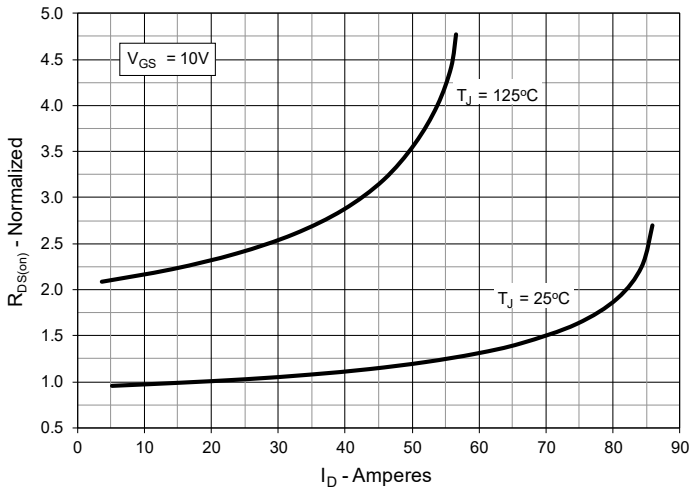
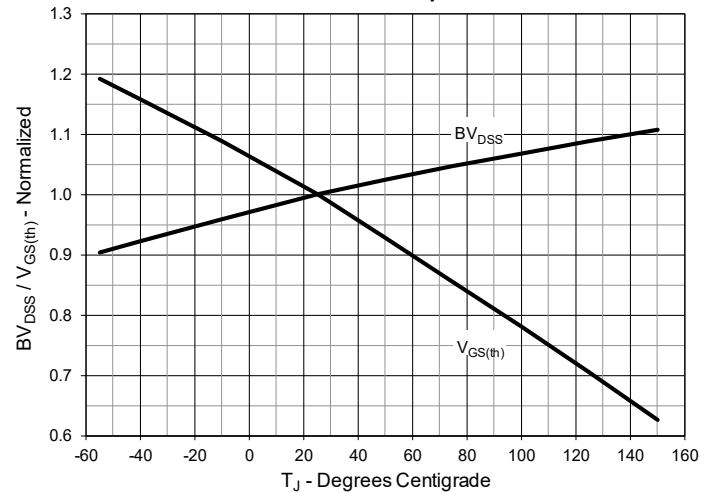
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 18\text{A}$ Value vs. Junction Temperature

Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 18\text{A}$ Value vs. Drain Current

Fig. 6. Normalized Breakdown & Threshold Voltages vs. Junction Temperature


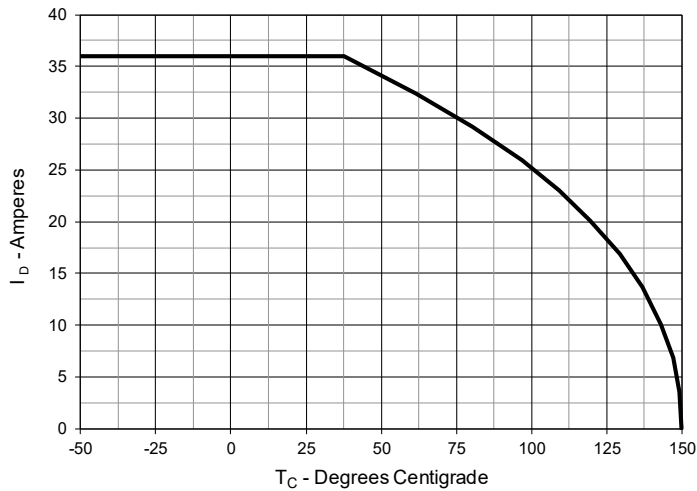
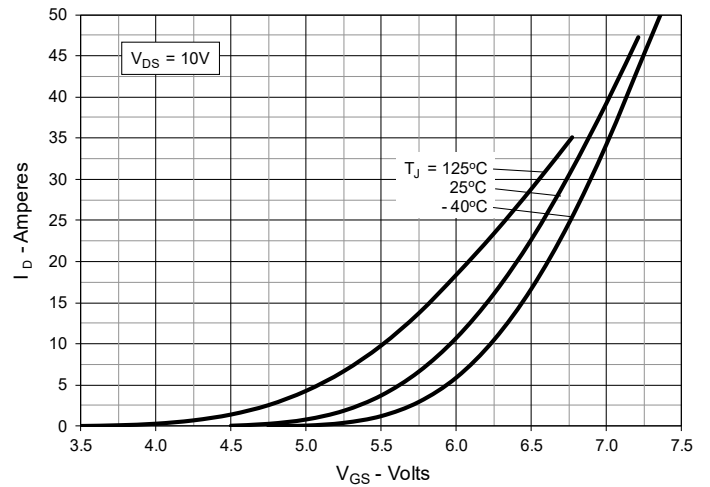
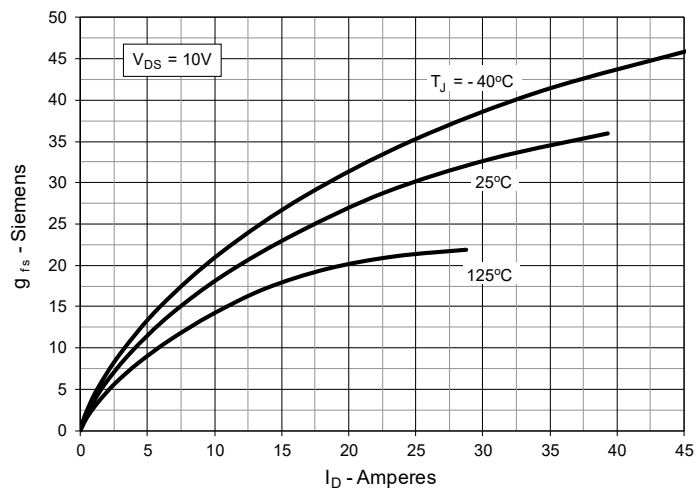
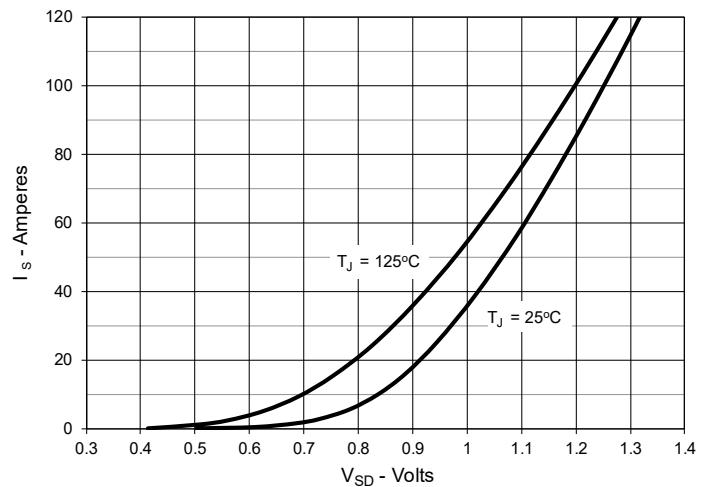
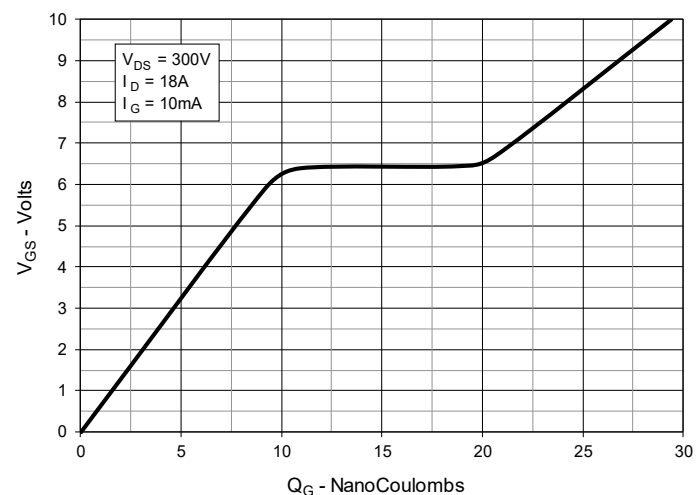
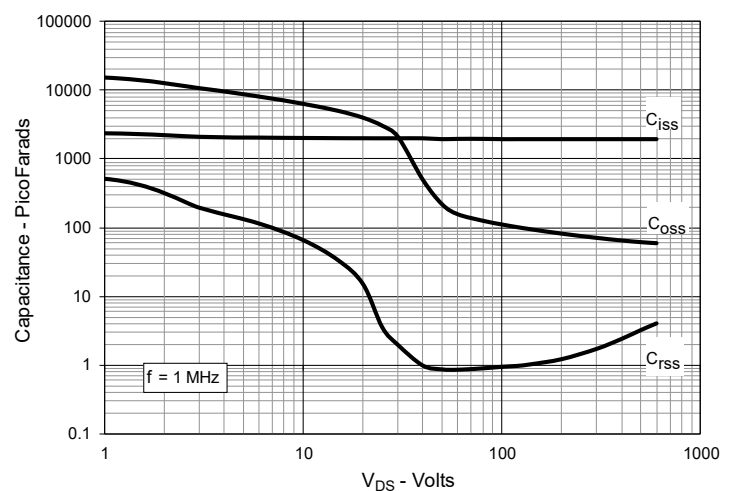
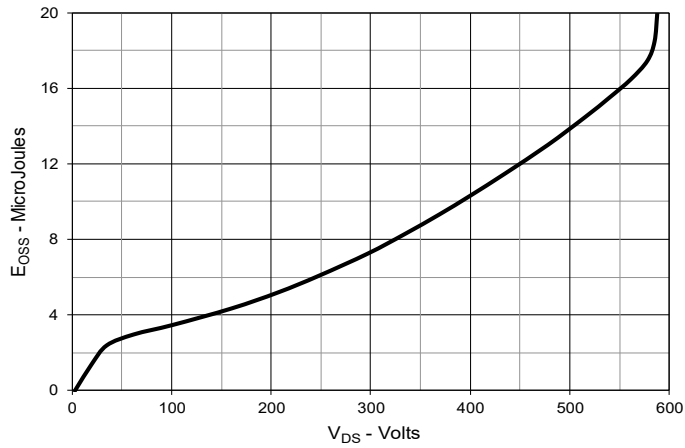
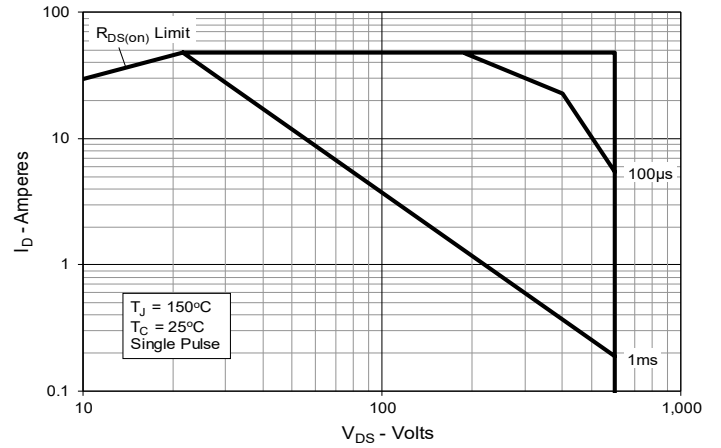
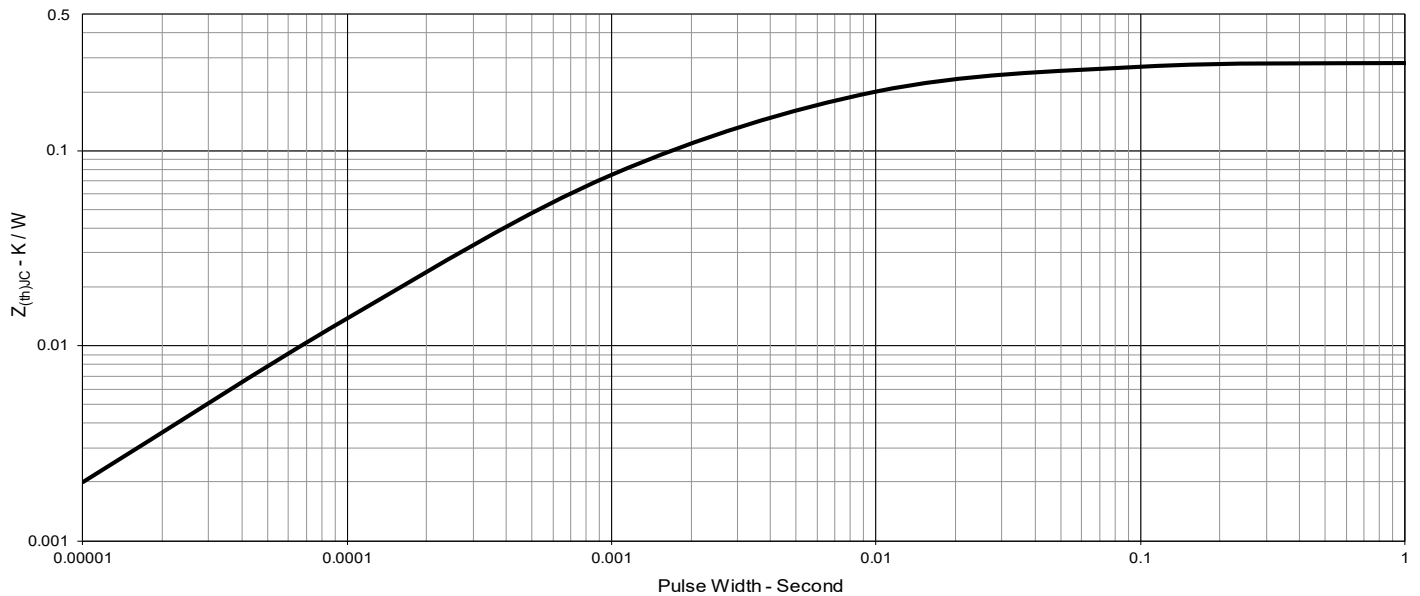
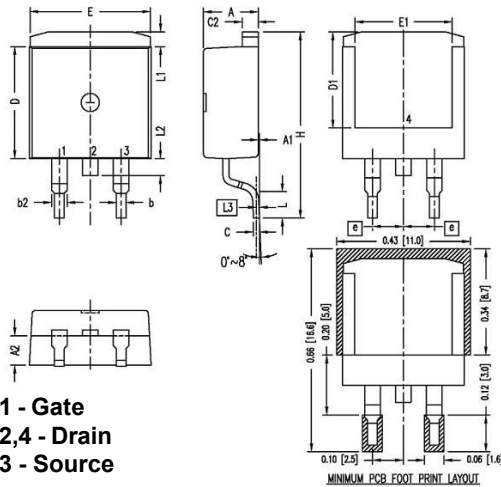
Fig. 7. Maximum Drain Current vs. Case Temperature

Fig. 8. Input Admittance

Fig. 9. Transconductance

Fig. 10. Forward Voltage Drop of Intrinsic Diode

Fig. 11. Gate Charge

Fig. 12. Capacitance


Fig. 13. Output Capacitance Stored Energy

Fig. 14. Forward-Bias Safe Operating Area

Fig. 15. Maximum Transient Thermal Impedance


TO-263 Outline


SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	.170	.185	4.30	4.70
A1	.000	.008	0.00	0.20
A2	.091	.098	2.30	2.50
b	.028	.035	0.70	0.90
b2	.046	.060	1.18	1.52
C	.018	.024	0.45	0.60
C2	.049	.060	1.25	1.52
D	.340	.370	8.63	9.40
D1	.300	.327	7.62	8.30
E	.380	.410	9.65	10.41
E1	.270	.330	6.86	8.38
e	.100	BSC	2.54	BSC
H	.580	.620	14.73	15.75
L	.075	.105	1.91	2.67
L1	.039	.060	1.00	1.52
L2		.070		1.77
L3	.010	BSC	0.254	BSC

NOTE:

1. This drawing meets all dimensions requirement of JEDEC outlines TO-263AB.
2. All metal surface are matte pure tin plated except trimmed area.
3.  is Gauge plane to measure L.
4. These dimension do not include mold flash and they will not exceed 0.005[0.13] per side.

