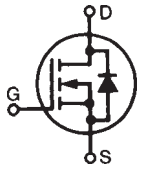
IXYS

Polar™ HiPerFET™ Power MOSFET

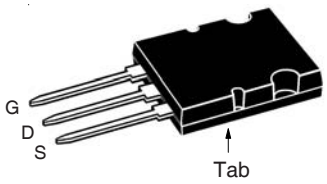
IXFB300N10P

V_{DSS} = 100V
I_{D25} = 300A
$R_{DS(on)}$ ≤ 5.5mΩ
t_{rr} ≤ 200ns

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



PLUS264™



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 175°C	100	V
V_{DGR}	T_J = 25°C to 175°C, R_{GS} = 1MΩ	100	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	300	A
I_{LRMS}	Leads Current Limit, RMS	160	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	900	A
I_A	T_C = 25°C	100	A
E_{AS}	T_C = 25°C	3	J
dv/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 175°C$	20	V/ns
P_D	T_C = 25°C	1500	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +175	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
F_C	Mounting Force	30..120/6.7..27	N/lb
Weight		10	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 3mA	100			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8mA	2.5		5.0	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			25	μA
	T_J = 150°C			1.5	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 50A, Note 1			5.5	mΩ

Features

- Low $R_{DS(on)}$ and Q_G
- Avalanche Rated
- Low Package Inductance
- Fast Intrinsic Diode

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- DC-DC Coverters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- DC Choppers
- AC and DC Motor Drives
- Uninterrupted Power Supplies
- High Speed Power Switching Applications

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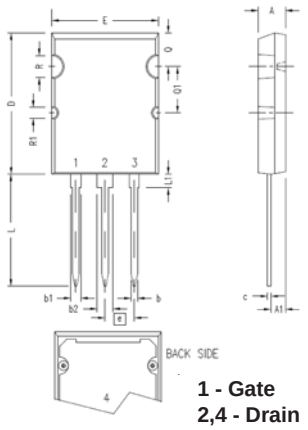
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10V, I_D = 60A, Note 1	55	92		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		23		nF
C_{oss}			6100		pF
C_{rss}			417		pF
$t_{d(on)}$	**Resistive Switching Times**		36		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 100A		35		ns
$t_{d(off)}$	R_G = 1Ω (External)		56		ns
t_f			25		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		279		nC
Q_{gs}			84		nC
Q_{gd}			107		nC
R_{thJC}				0.10	°C/W
R_{thCS}			0.13		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			300	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			1000	A
V_{SD}	I_F = 100A, V_{GS} = 0V, Note 1			1.3	V
t_{rr}	I_F = 150A, -di/dt = 100A/μs			200	ns
Q_{RM}	V_R = 50V		0.71		μC
I_{RM}			10		A

Note 1: Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

PLUS264™ (IXFB) Outline



1 - Gate
2,4 - Drain
3 - Source

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215 BSC		5.46 BSC	
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
ØR	.155	.187	3.94	4.75
ØR1	.085	.093	2.16	2.36

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Extended Output Characteristics @ T_J = 25ºC

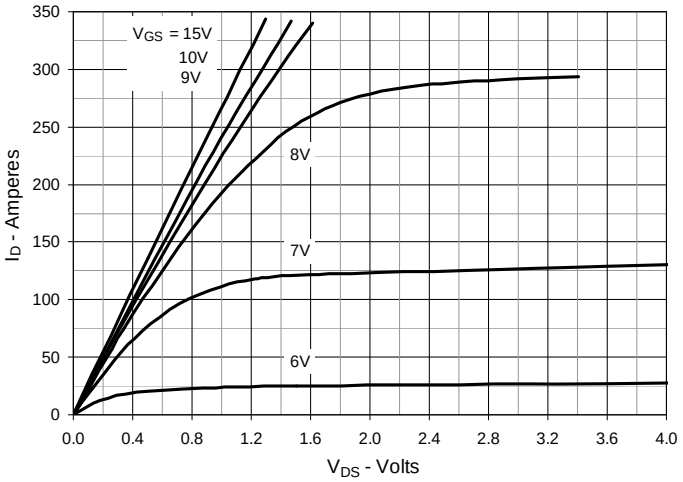


Fig. 2. Output Characteristics @ T_J = 150ºC

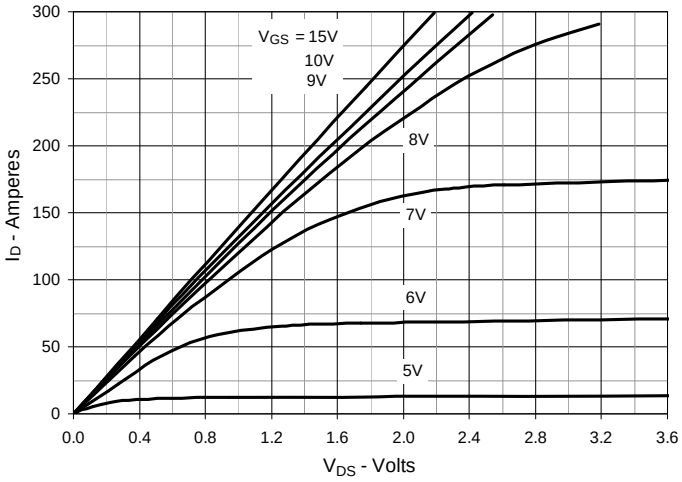


Fig. 3. $R_{DS(on)}$ Normalized to I_D = 150A Value vs. Junction Temperature

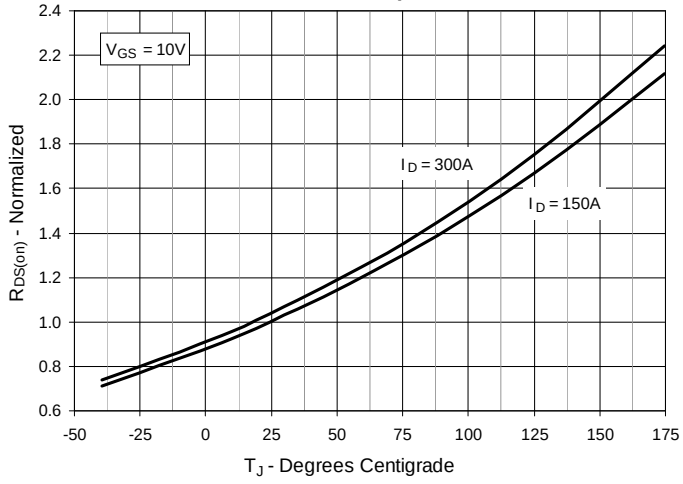


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 150A Value vs. Drain Current

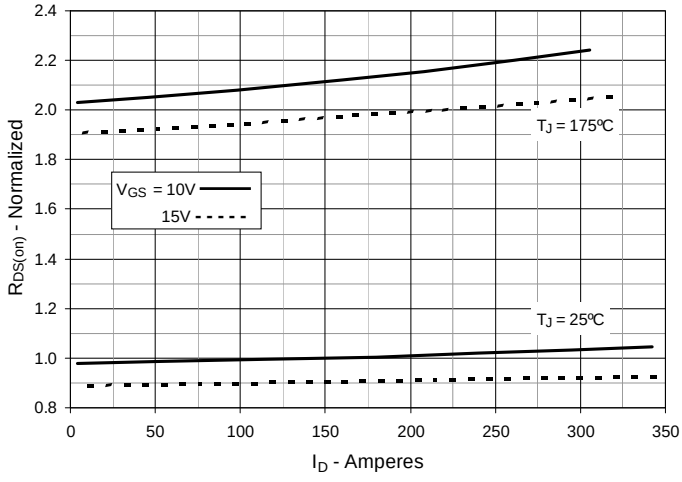


Fig. 5. Maximum Drain Current vs. Case Temperature

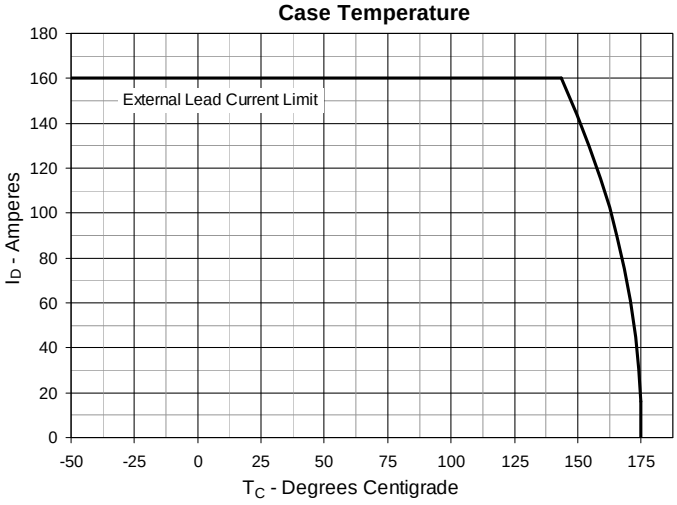
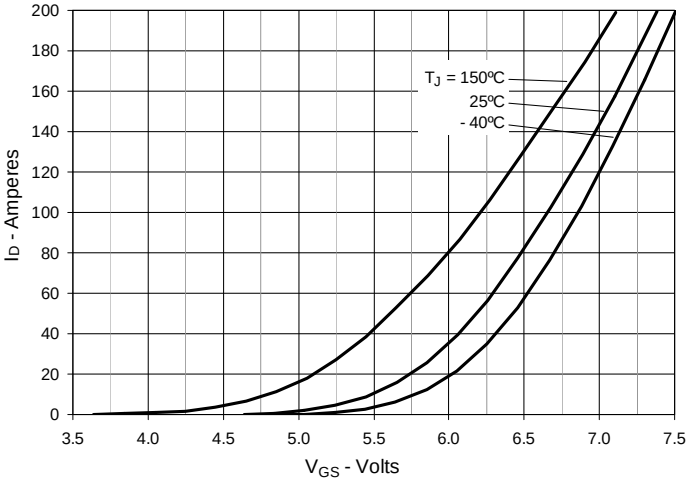


Fig. 6. Input Admittance



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Fig. . Transconductance

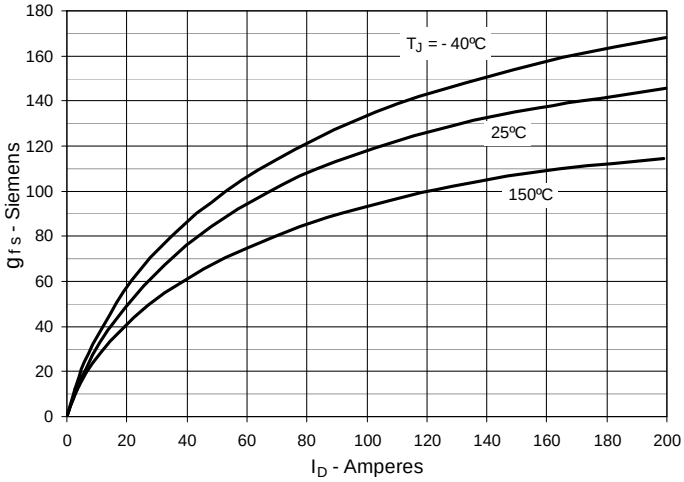


Fig. 8. Forward Voltage Drop of Intrinsic Diode

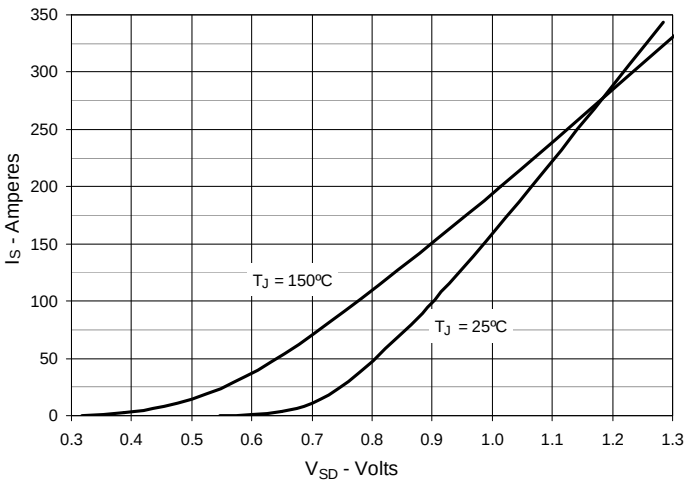


Fig. 9. Gate Charge

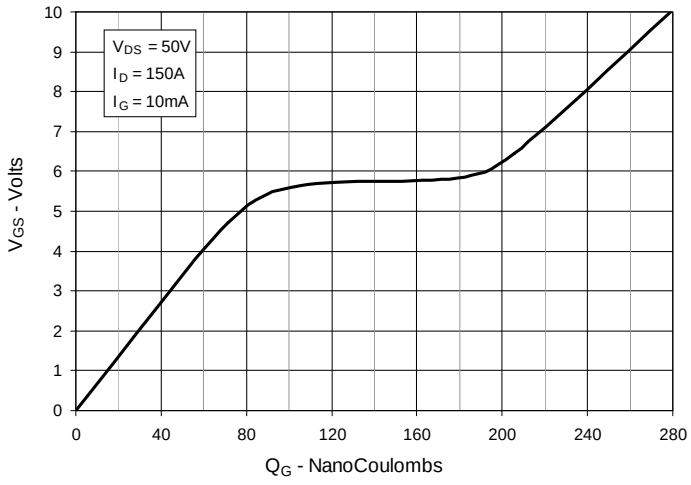


Fig. 10. Capacitance

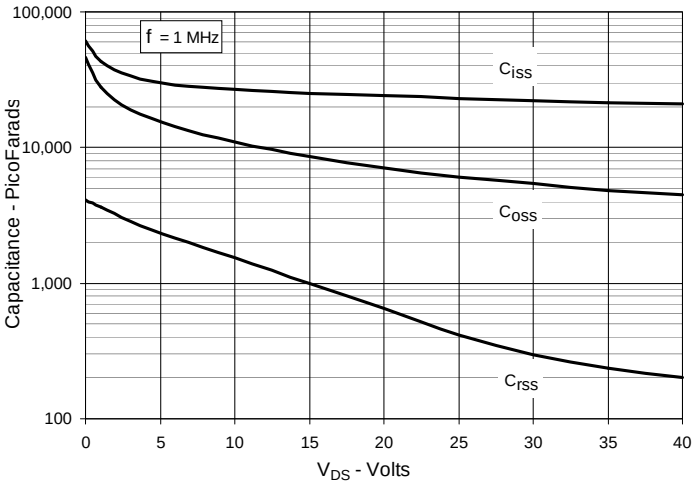


Fig. 11. Forward-Bias Safe Operating Area

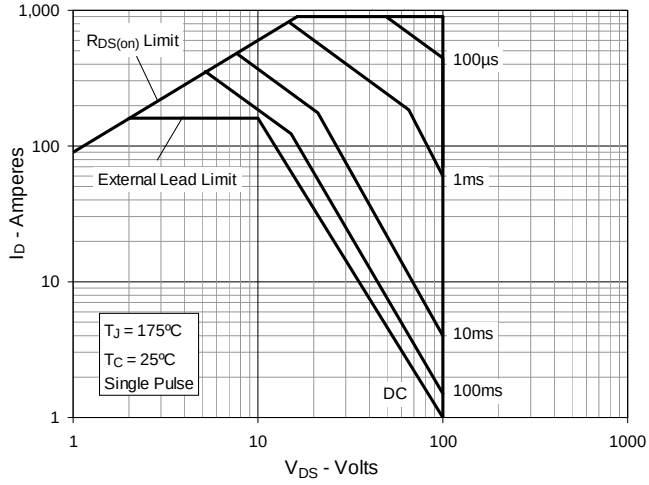
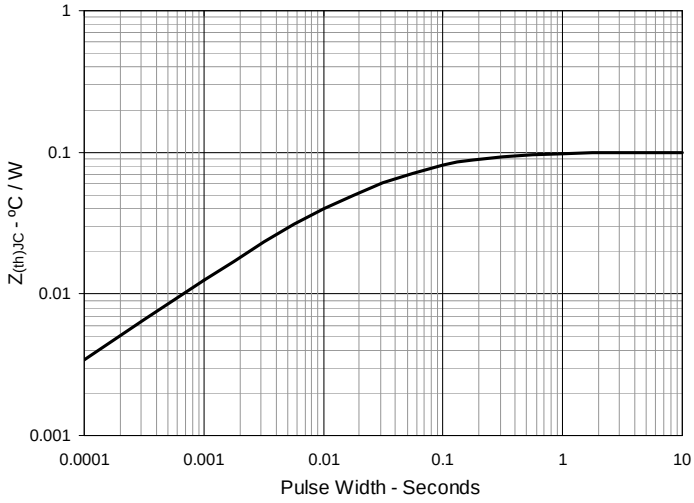


Fig. 12. Maximum Transient Thermal Impedance



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