IXYS
A Littelfuse Technology

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Symmetrical Gate Turn-Off Thyristor
Types S0700KC14# to S0700KC17#

Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	1400-1700	V
V_{DSM}	Non-repetitive peak off-state voltage, (note 1)	1500-1800	V
V_{RRM}	Repetitive peak reverse voltage	100-1400	V
V_{RSM}	Non-repetitive peak reverse voltage	100-1400	V

	RATINGS	MAXIMUM LIMITS	UNITS
I_{TGQ}	Peak turn-off current, (note 2)	700	A
L_s	Snubber loop inductance, $I_{TM}=I_{TGQ}$, (note 2)	0.3	µH
$I_{T(AVM)}$	Mean on-state current, T_{sink}=55°C (note 3)	430	A
$I_{T(RMS)}$	Nominal RMS on-state current, 25°C (note 3)	870	A
I_{TSM}	Peak non-repetitive surge current t_p=10ms	5	kA
I_{TSM2}	Peak non-repetitive surge current, (Note 4)	9	kA
I^2t	I^2t capacity for fusing t_p=10ms	125×10^3	A^2s
di/dt_{cr}	Critical rate of rise of on-state current, (note 5)	1000	A/µs
P_{FGM}	Peak forward gate power	160	W
P_{RGM}	Peak reverse gate power	5	kW
I_{FGM}	Peak forward gate current	100	A
V_{RGM}	Peak reverse gate voltage (note 6).	18	V
t_{off}	Minimum permissible off-time, $I_{TM}=I_{TGQ}$, (note 2)	70	µs
t_{on}	Minimum permissible on-time	20	µs
$T_{j\,op}$	Operating temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-40 to +150	°C

Notes:-
1) V_{GK}=-2Volts.
2) T_j=125°C, V_D=80%V_{DM}, V_{DM}<V_{DRM}, di_{GQ}/dt=20A/µs, $I_{TM}=I_{TGQ}$ & C_S=1.5µF.
3) Double-side cooled, single phase; 50Hz, 180° half-sinewave.
4) Half-sinewave, t_p=2ms
5) For di/dt >1000A/µs, consult factory.
6) May exceed this value during turn-off avalanche period.

Characteristics

	Parameter	MIN	TYP	MAX	TEST CONDITIONS	UNITS
V_{TM}	Maximum peak on-state voltage	-	1.9	2.2	I_G=1.5A, I_T=700A	V
I_L	Latching current	-	5	-	T_j=25°C	A
I_H	Holding current.	-	5	-	T_j=25°C	A
dv/dt_{cr}	Critical rate of rise of off-state voltage	800	-	-	V_D=80%V_{DRM}, V_{GR}=-2V	V/µs
I_{DM}	Peak off state current	-	-	30	Rated V_{DRM}, V_{GR}=-2V	mA
I_{RM}	Peak reverse current	-	-	40	Rated V_{RRM}	mA
I_{GKM}	Peak negative gate leakage current	-	-	200	V_{GR}=-16V	mA
V_{GT}	Gate trigger voltage	-	0.9	-	T_j=-40°C	V
		-	0.8	-	T_j=25°C V_D=25V, R_L=25mΩ	V
		-	0.7	-	T_j=125°C	V
I_{GT}	Gate trigger current	-	1.5	6	T_j=-40°C	A
		-	0.5	1	T_j=25°C V_D=25V, R_L=25mΩ	A
		-	125	400	T_j=125°C	mA
t_d	Delay time	-	0.8	-	V_D=50%V_{DRM}, I_{TGQ}=700A, I_{GM}=12A, di_G/dt=6A/µs T_j=25°C, di/dt=300A/µs, (10%I_{GM} to 90%V_D)	µs
t_{gt}	Turn-on time	-	3	5	Conditions as for t_d, (10%I_{GM} to 10%V_D)	µs
t_f	Fall time	-	0.8	-	V_D=50%V_{DRM}, I_{TGQ}=700A, C_S=1.5µF, di_{GQ}/dt=20A/µs, V_{GR}=-16V, (90%I_{TGQ} to 10%I_{TGQ})	µs
t_{gq}	Turn-off time	-	10	11	Conditions as for t_f, (10%I_{GQ} to 10%I_{TGQ})	µs
I_{gq}	Turn-off gate current	-	190	-	Conditions as for t_f	A
Q_{gq}	Turn-off gate charge	-	1.3	1.45	Conditions as for t_f	mC
t_{tail}	Tail time	-	30	50	Conditions as for t_f, (10%I_{TGQ} to I_{TGQ}<1A)	µs
t_{gw}	Gate off-time (see note 3).	100	-	-	Conditions as for t_f	µs
R_{thJK}	Thermal resistance junction to sink	-	-	0.063	Double side cooled	K/W
		-	-	0.21	Cathode side cooled	K/W
		-	-	0.09	Anode side cooled	K/W
F	Mounting force	4.5	-	9.0	(see note 2)	kN
W_t	Weight	-	120	-		g

Notes:-
1) Unless otherwise indicated T_j=125°C.
2) For other clamping forces, consult factory.
3) The gate off-time is the period during which the gate circuit is required to remain low impedance to allow for the passage of tail current.

Notes on ratings and characteristics.

1. Maximum Ratings.

1.1 Off-state voltage ratings.

Unless otherwise indicated, all off-state voltage ratings are given for gate conditions as diagram 1. For other gate conditions see the curves of figure 5. It should be noted that V_{DRM} is the repeatable peak voltage which may be applied to the device and does not relate to a DC operating condition. While not given in the ratings, V_{DC} should ideally be limited to 60% V_{DRM} in this product.

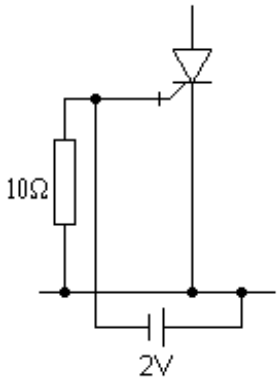


Diagram 1.

1.2 Reverse voltage rating.

All devices in this series have a minimum V_{RRM} of 100 Volts. If specified at the time of order, a V_{RRM} up to 80%V_{DRM} is available.

1.3 Peak turn-off current.

The figure given in maximum ratings is the highest value for normal operation of the device under conditions given in note 2 of ratings. For other combinations of I_{TGQ}, V_D and C_s see the curves of figures 15 & 16. The curves are effective over the normal operating range of the device and assume a snubber circuit equivalent to that given in diagram 2. If a more complex snubber, such as an Underland circuit, is employed then the equivalent C_S should be used and L_s<0.3µH must be ensured for the curves to be applied.

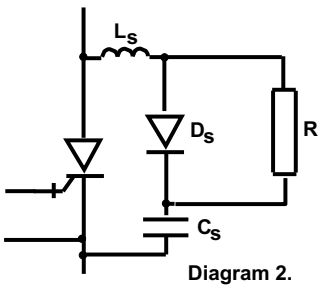


Diagram 2.

1.4 R.M.S and average current.

Measured as for standard thyristor conditions, double side cooled, single phase, 50Hz, 180° half-sinewave. These are included as a guide to compare the alternative types of GTO thyristors available, values can not be applied to practical applications, as they do not include switching losses.

1.5 Surge rating and I^2t.

Ratings are for half-sinewave, peak value against duration is given in the curve of figure 4.

1.6 Snubber loop inductance.

Use of GTO thyristors with snubber loop inductance, L_s<0.3µH implies no dangerous V_s voltages (see diagrams 2 & 3) can be applied, provided the other conditions given in note 1.3 are enforced. Alternatively, V_s should be limited to 600 Volts to avoid possible device failure.

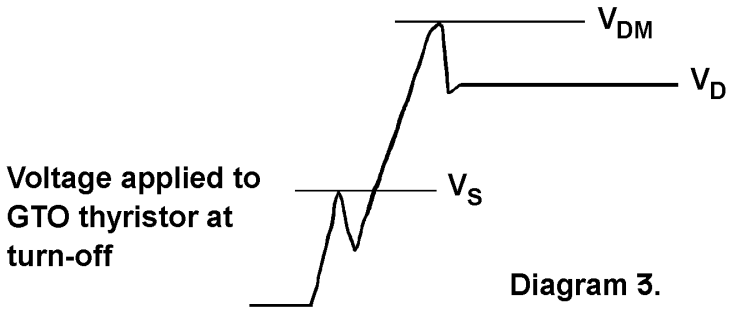


Diagram 3.

1.7 Critical rate of rise of on-state current

The value given is the maximum repetitive rating but does not imply any specific operating condition. The high turn-on losses associated with limit di/dt would not allow for practical duty cycle at this maximum condition. For special pulse applications, such as crowbars and pulse power supplies, a much higher di/dt is possible. Where the device is required to operate with infrequent high current pulses, with natural commutation (i.e. not gate turn-off), then di/dt>3kA/µs is possible. For this type of operation individual specific evaluation is required.

1.8 Gate ratings

The absolute conditions above which the gate may be damaged. It is permitted to allow $V_{GK(AV)}$ during turn-off (see diagram 10) to exceed V_{RGM} which is the implied DC condition.

1.9 Minimum permissible off time.

This time relates specifically to re-firing of device (see also note on gate-off time 2.7). The value given in the ratings applies only to operating conditions of ratings note 2. For other operating conditions see the curves of figure 18.

1.10 Minimum permissible on-time.

Figure is given for minimum time to allow complete conduction of all the GTO thyristor islands. Where a simple snubber, of the form given in diagram 1. (or any other non-energy recovery type which discharges through the GTO at turn-on) the actual minimum on-time will usually be fixed by the snubber circuit time constant, which must be allowed to fully discharge before the GTO thyristor is turned off. If the anode circuit has di/dt<10A/µs then the minimum on-time should be increased, the actual value will depend upon the di/dt and operating conditions (each case needs to be assessed on an individual basis).

2 Characteristics

2.1 Instantaneous on-state voltage

Measured using a 500µs square pulse, see also the curves of figure 2 for other values of I_{TM}.

2.2 Latching and holding current

These are considered to be approximately equal and only the latching current is measured, type test only as outlined below. The test circuit and wave diagrams are given in diagram 4. The anode current is monitored on an oscilloscope while V_D is increased, until the current is seen to flow during the un-gated period between the end of I_G and the application of reverse gate voltage. Test frequency is 100Hz with I_{GM} & I_G as for t_d of characteristic data.

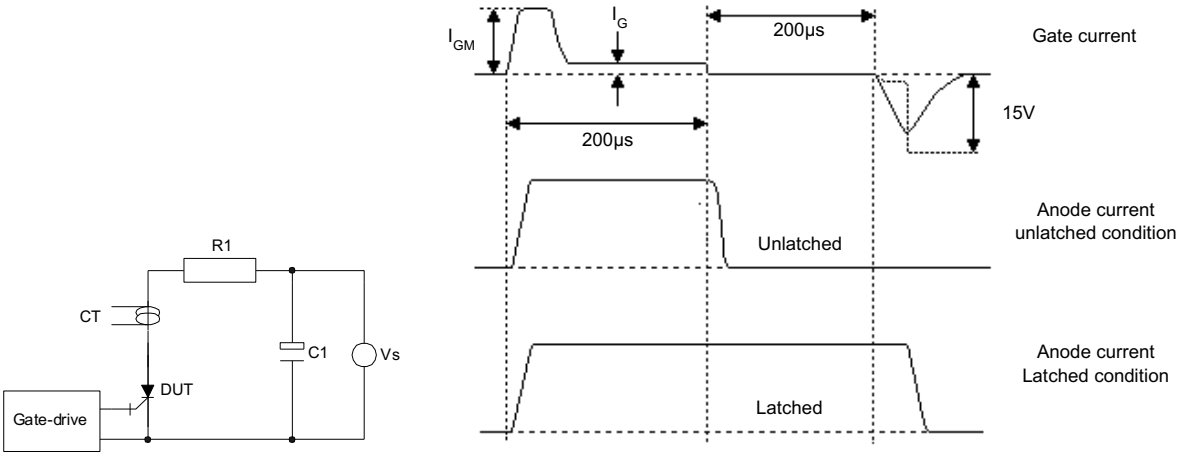


Diagram 4, Latching test circuit and waveforms.

2.3 Critical dv/dt

The gate conditions are the same as for 1.1, this characteristic is for off-state only and does not relate to dv/dt at turn-off. The measurement, type test only, is conducted using the exponential ramp method as shown in diagram 5. It should be noted that GTO thyristors have a poor static dv/dt capability if the gate is open circuit or R_{GK} is high impedance. Typical values: - dv/dt<30V/µs for R_{GK}>10Ω.

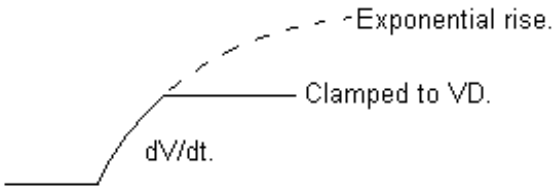


Diagram 5, Definition of dV/dt.

2.4 Off-state leakage.

For I_{DRM} & I_{RRM} see notes 1.1 & 1.2 for gate leakage I_{GK}, the off-state gate circuit is required to sink this leakage and still maintain minimum of –2 Volts. See diagram 6.

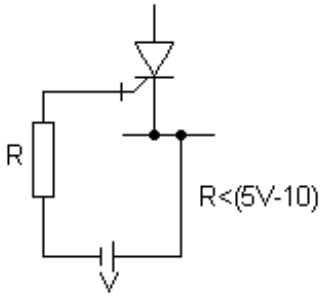


Diagram 6.

2.5 Gate trigger characteristics.

These are measured by slowly ramping up the gate current and monitoring the transition of anode current and voltage (see diagram 7). Maximum and typical data of gate trigger current, for the full junction temperature range, is given in the curves of figure 6. Only typical figures are given for gate trigger voltage, however, the curves of figure 1 give the range of gate forward characteristics, for the full allowable junction temperature range. The curves of figures 1 & 6 should be used in conjunction, when considering forward gate drive circuit requirement. The gate drive requirements should always be calculated for the lowest junction temperature start-up condition.

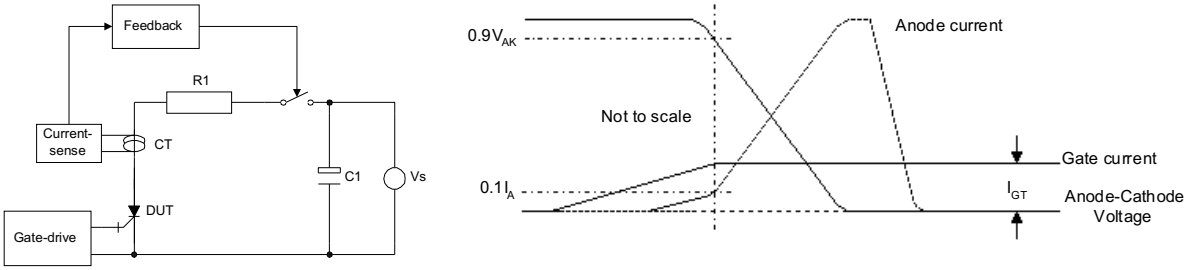


Diagram 7, Gate trigger circuit and waveforms.

2.6 Turn-on characteristics

The basic circuit used for turn-on tests is given in diagram 8. The test is initiated by establishing a circulating current in T_x, resulting in V_D appearing across C_c/L_c. When the test device is fired C_c/L_c discharges through DUT and commutates T_x off, as pulse from C_c/L_c decays the constant current source continues to supply a fixed current to DUT. Changing value of C_c & L_c allows adjustment of I_{TM} and di/dt respectively, V_D and i are also adjustable.

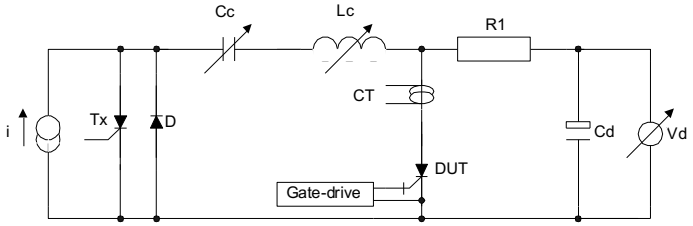


Diagram 8, Turn-on test circuit of FT40.

The definitions of turn-on parameters used in the characteristic data are given in diagram 9. The gate circuit conditions I_{GM} & I_G are fully adjustable, I_{GM} duration 10µs.

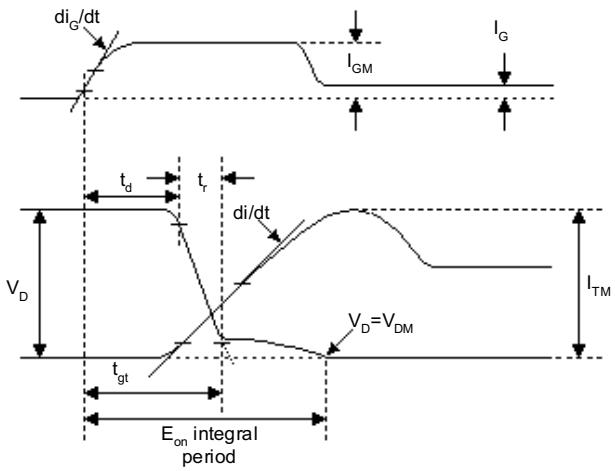


Diagram 9, Turn-on wave-diagrams.

In addition to the turn-on time figures given in the characteristics data, the curves of figure 9 give the relationship of t_{gt} to di/dt and I_{GM}. The data in the curves of figures 7 & 8, gives the turn-on losses both with and without snubber discharge, a snubber of the form given in diagram 2 is assumed. Only typical losses are given due to the large number of variables which effect E_{on}. It is unlikely that all negative aspects would appear in any one application, so typical figures can be considered as worst case. Where the turn-on loss is higher than the figure given it will in most cases be compensated by reduced turn-off losses, as variations in processing inversely effect many parameters. For a worst-case device, which would also have the lowest turn-off losses, E_{on} would be 1.5x values given in the curves of figures 7 & 8. Turn-on losses are measured over the integral period specified below: -

$$Eon = \int_0^{10\mu s} iv.dt$$

The turn-on loss can be sub-divided into two component parts, firstly that associated with t_{gt} and secondly the contribution of the voltage tail. For this series of devices t_{gt} contributes 50% and the voltage tail 50% (These figures are approximate and are influenced by several second order effects). The loss during t_{gt} is greatly affected by gate current and as with turn-on time (figure 9), it can be reduced by increasing I_{GM}. The turn-on loss associated with the voltage tail is not effected by the gate conditions and can only be reduced by limiting di/dt, where appropriate a turn-on snubber should be used. In applications where the snubber is discharged through the GTO thyristor at turn-on, selection of discharge resistor will effect E_{on}. The curves of figure 8 are given for a snubber as shown in diagram 2, with R=5Ω, this is the lowest recommended value giving the highest E_{on}, higher values will reduce E_{on}.

2.7 Turn-off characteristics

The basic circuit used for the turn-off test is given in diagram 10. Prior to the negative gate pulse being applied constant current, equivalent to I_{TGQ}, is established in the DUT. The switch S_x is opened just before DUT is gated off with a reverse gate pulse as specified in the characteristic/data curves. After the period t_{gt} voltage rises across the DUT, dv/dt being limited by the snubber circuit. Voltage will continue to rise across DUT until D_c turns-on at a voltage set by the active clamp C_c, the voltage will be held at this value until energy stored in L_x is depleted, after which it will fall to V_{DC}. The value of L_x is selected to give required V_D Over the full tail time period. The overshoot voltage V_{DM} is derived from L_c and forward voltage characteristic of D_C, typically V_{DM}=1.2V_D to 1.5V_D depending on test settings. The gate is held reverse biased through a low impedance circuit until the tail current is fully extinguished.

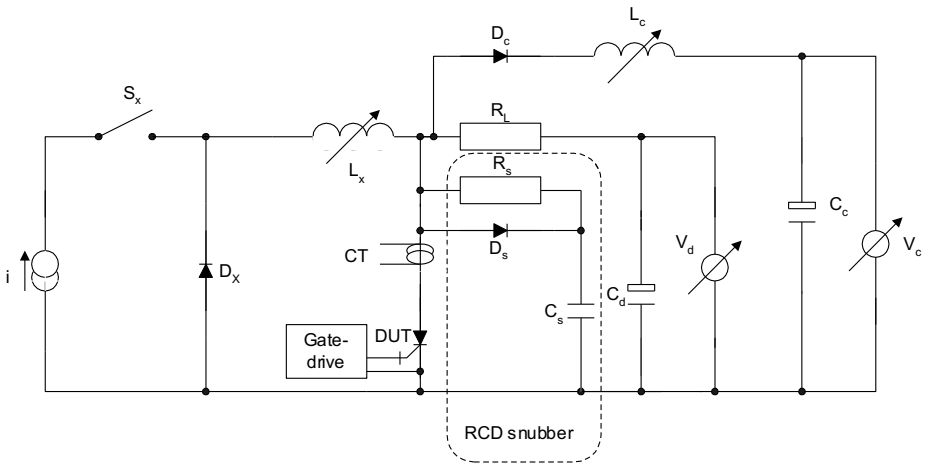


Diagram 10, Turn-off test circuit.

The definitions of turn-off parameters used in the characteristic data are given in diagram 11.

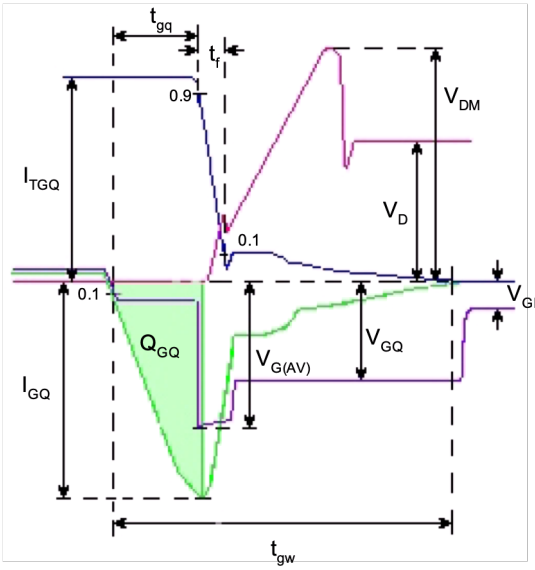


Diagram 11, Turn-off parameter definitions.

In addition to the turn-off figures given in characteristic data, the curves of figures 10, 11 & 12 give the relationship of I_{GQ} Q_{GQ} and t_{gq} to turn-off current (I_{TGQ}) and di_{GQ}/dt. Only typical values of I_{GQ} are given due to a great dependence upon the gate circuit impedance, which is a function of gate drive design not the device. The t_{gq} is also, to a lesser extent, affected by circuit impedance and as such the maximum figures given in data assume a good low impedance circuit design. The curves of figures 17 & 18 give the tail time and minimum off time to re-fire device as a function of turn-off current. The minimum off time to re-fire the device is distinct from t_{gw}, the gate off time given in characteristics. The GTO thyristor may be safely re-triggered when a small amount of tail current is still flowing. In contrast, the gate circuit must remain low impedance until the tail current has fallen to zero or below a level which the higher impedance V_{GR} circuit can sink without being pulled down below –2 Volts. If the gate circuit is to be switched to a higher impedance before the tail current has reached zero, then the requirements of diagram 12 must be applied.

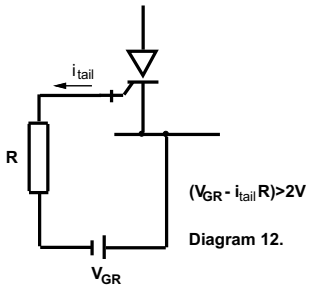


Diagram 12.

The figure t_{gw}, as given in the characteristic data, is the maximum time required for the tail current to decay to zero. The figure is applicable under all normal operating conditions for the device; provided suitable gate drive is employed. At lower turn-off current, or with special gate drive considerations, this time may be reduced (each case needs to be considered individually). Typical turn-off losses are given in the curves of figures 13 & 14, the integration period for the losses is nominally taken to the end of the tail time (I_{tail}<1A) i.e. :-

$$Eoff = \int_{0}^{tgt+ttail} iv.dt.$$

The curves of figure 13 give the turn-off energy for a fixed V_D with a V_{DM}=120%V_D, whereas the curves of figure 14 give the turn-off energy with a fixed value of V_{DM} and V_D=50%V_{DRM}. The curves are for energy against turn-off current/snubber capacitance with a correction for voltage inset as an additional graph (snubber equivalent to diagram 2 is assumed). From these curves a typical value of turn-off energy for any combination of I_{TGQ}/C_s and V_D or V_{DM} can be derived. Only typical data is included, to allow for the trade-off with on-state voltage (V_{TM}) which is a feature of these devices, see diagram 13. When calculating losses in an application, the use of a maximum V_{TM} and typical E_{off} will (under normal operating frequencies) give a more realistic value. The lowest V_{TM} device of this type would have a maximum turn-off energy of 1.5x the figure given in the curves of figures 13 & 14.

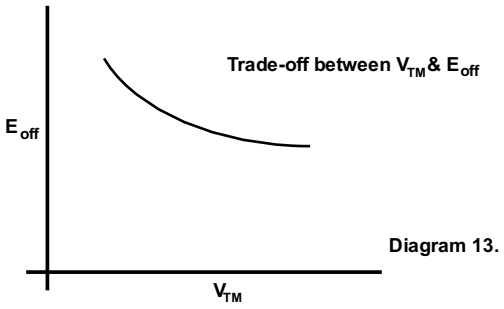


Diagram 13.

2.8 Safe turn-off periphery

The necessity to control dv/dt at tun-off for the GTO thyristor implies a trade-off between $I_{TGQ}/V_{DM}/C_s$. This information is given in the curves of figures 15 & 16. The information in these curves should be considered as maximum limits and not implied operating conditions, some margin of 'safety' is advised with the conditions of the curves reserved for occasional excursions. It should be noted that these curves are derived at maximum junction temperature, however, they may be applied across the full operating temperature range of the device provided additional precautions are taken. At very low temperature, (below –10°C) the fall-time of device becomes very rapid and can give rise to very high turn-off voltage spikes, as such it is advisable to reduce snubber loop inductance to <0.2µH to minimise this effect.

Curves

Figure 1 – Forward gate characteristics

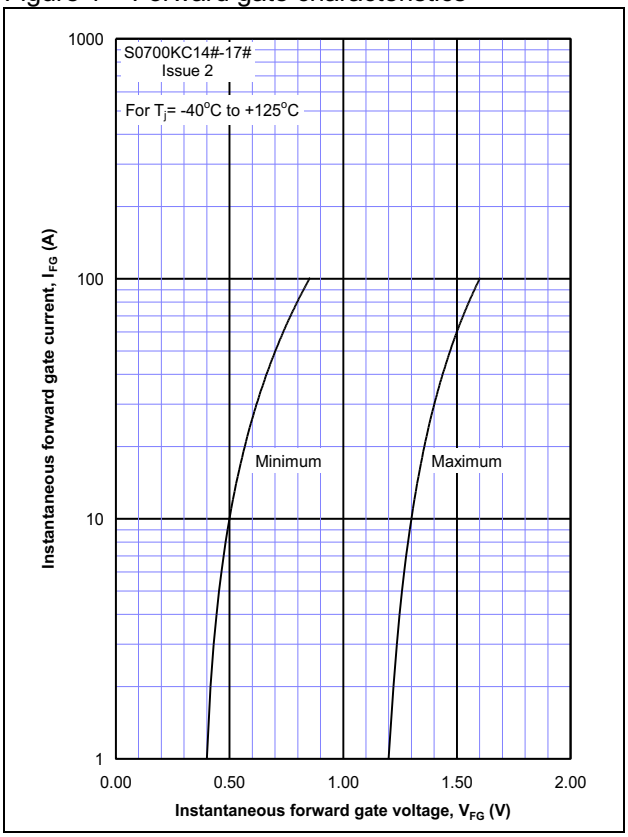


Figure 2 - On-state characteristics of Limit device

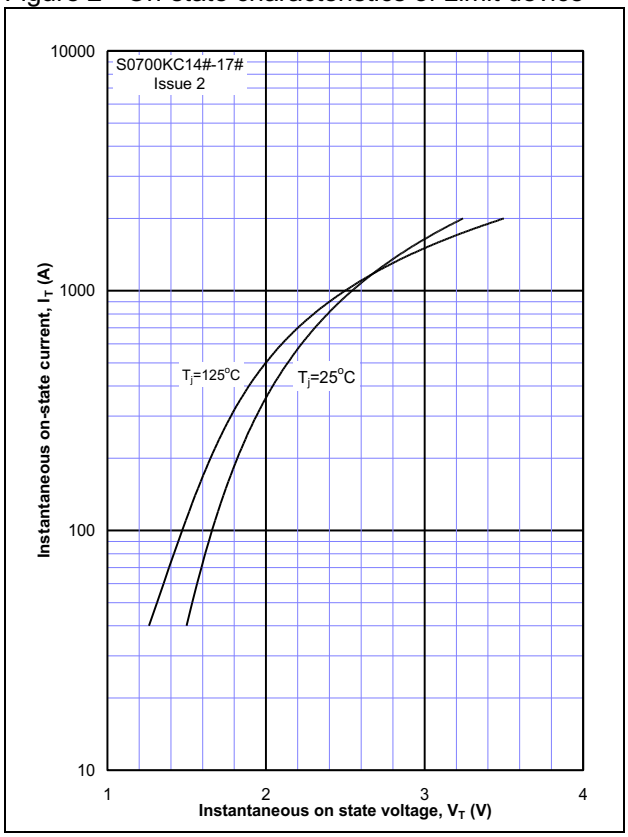


Figure 3 - Maximum surge and I^2t Ratings

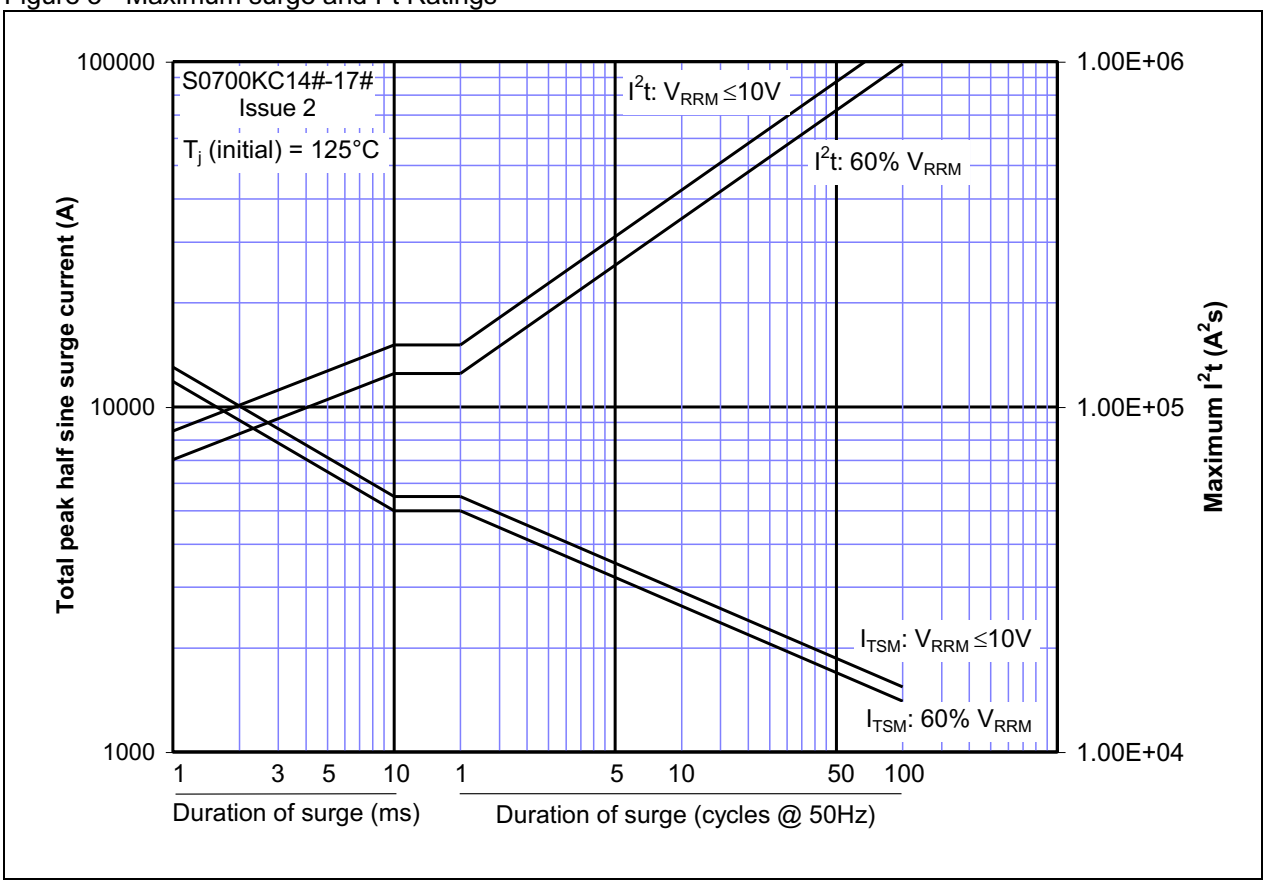


Figure 4 – Transient thermal impedance

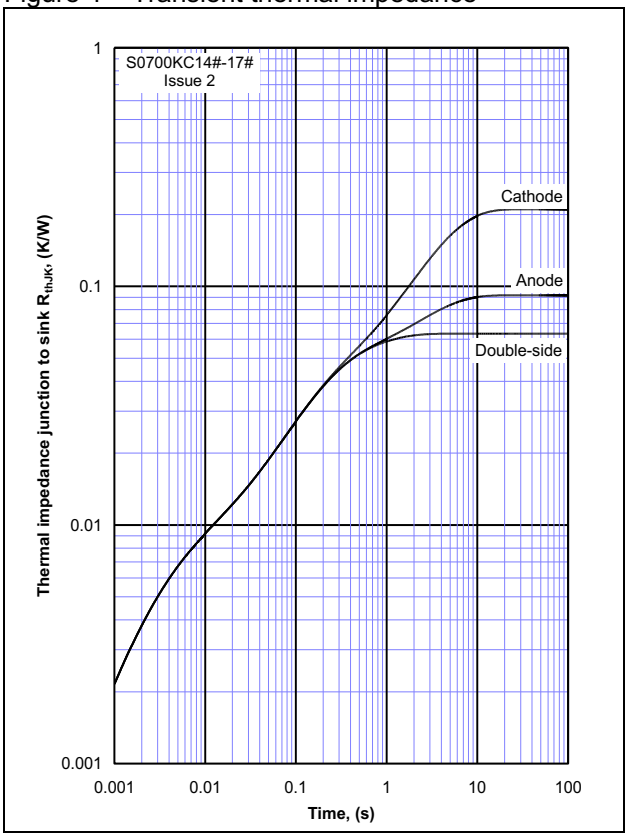


Figure 5 – Typical forward blocking voltage Vs. external gate-cathode resistance

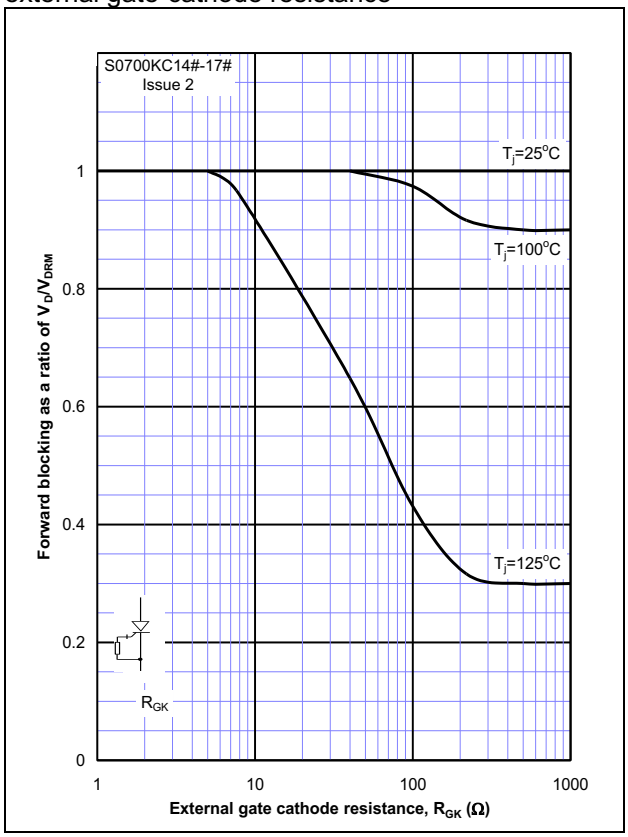


Figure 6 – Gate trigger current

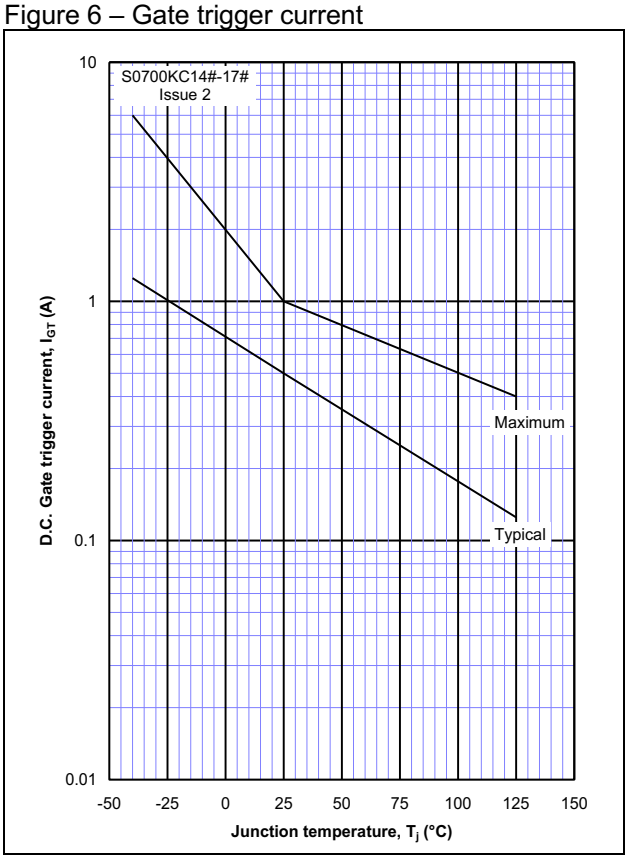


Figure 7 – Typical turn-on energy per pulse (excluding snubber discharge)

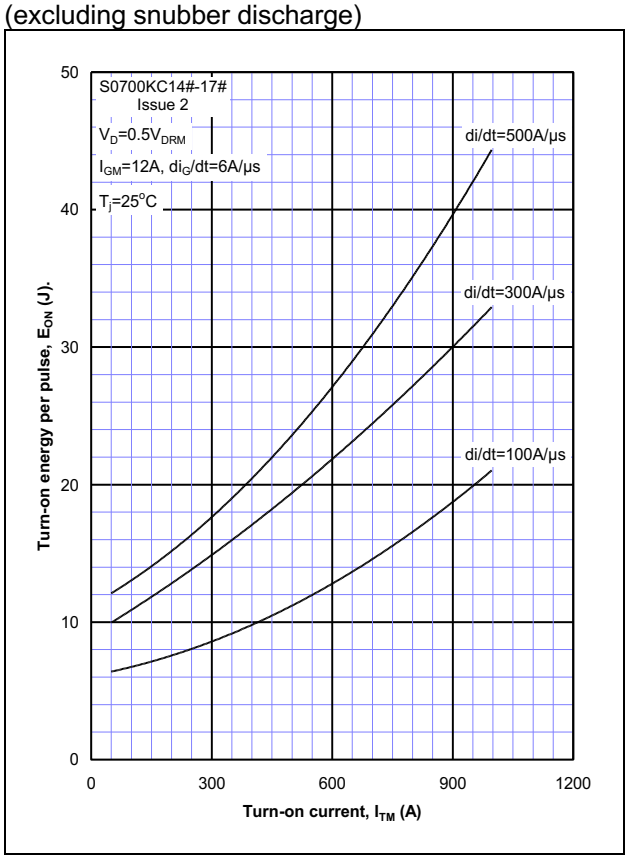


Figure 8 – Typical turn-on energy per pulse (including snubber discharge)

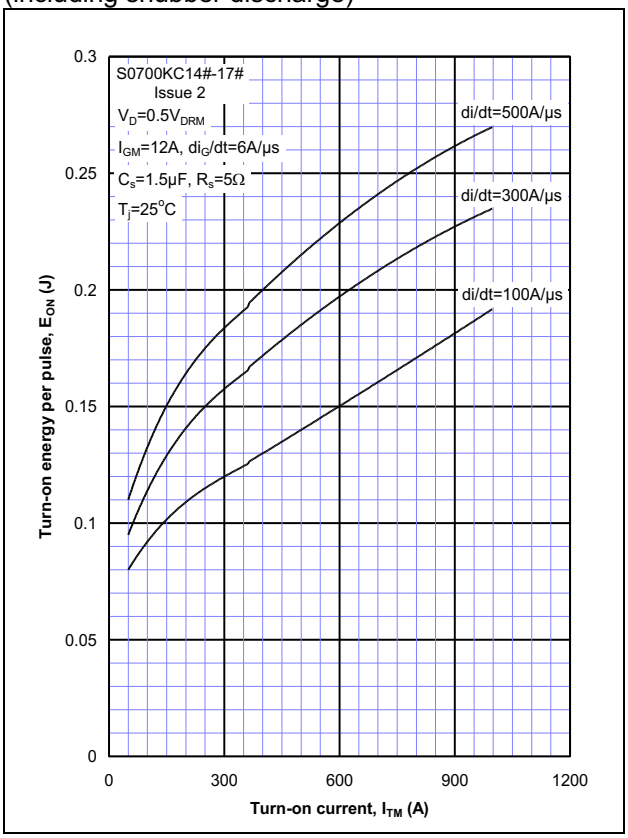


Figure 9 – Maximum turn-on time

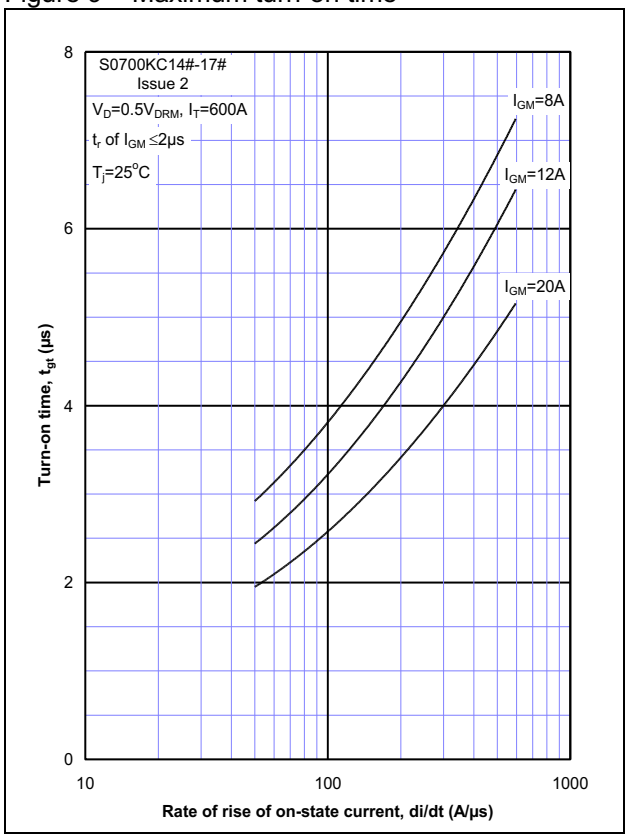


Figure 10 – Typical peak turn-off gate current

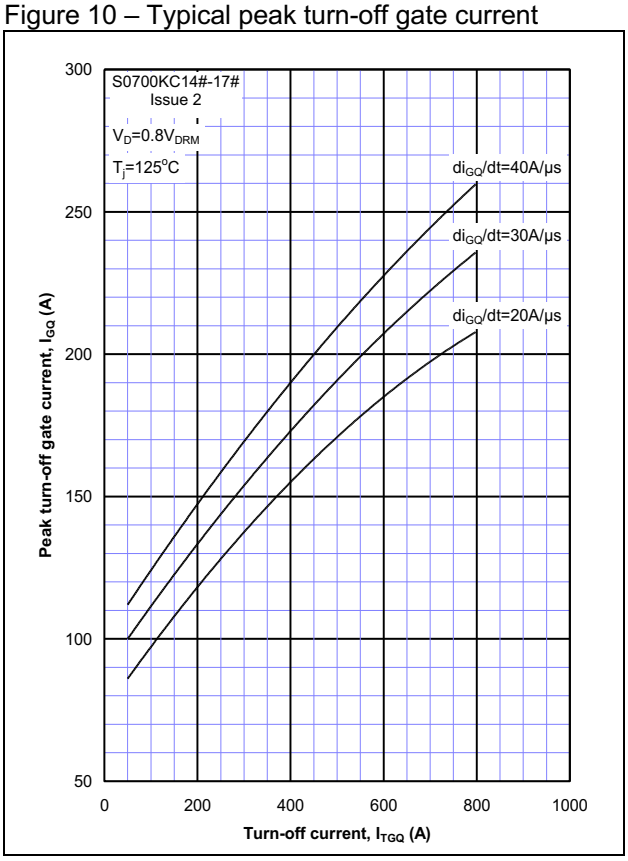


Figure 11 – Maximum gate turn-off charge

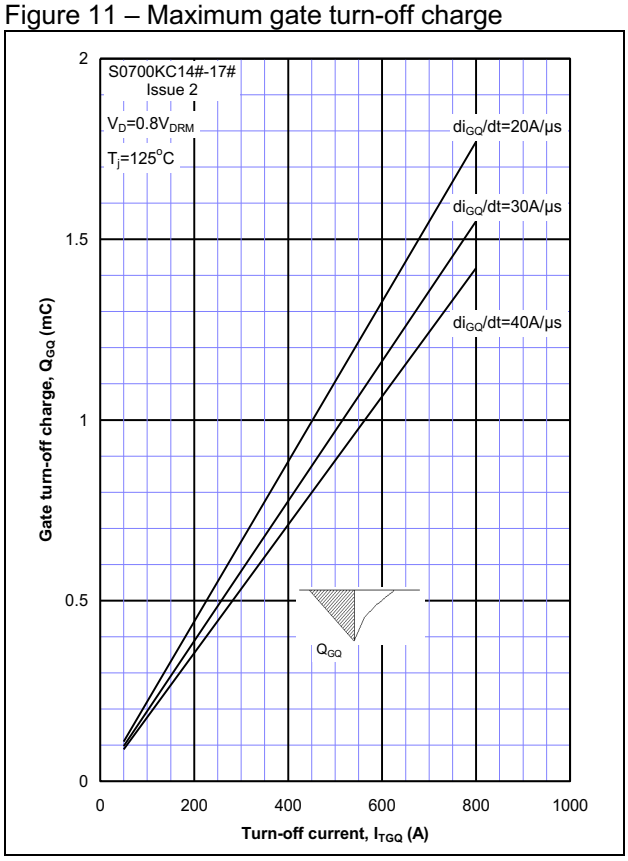


Figure 12 – Maximum turn-off time

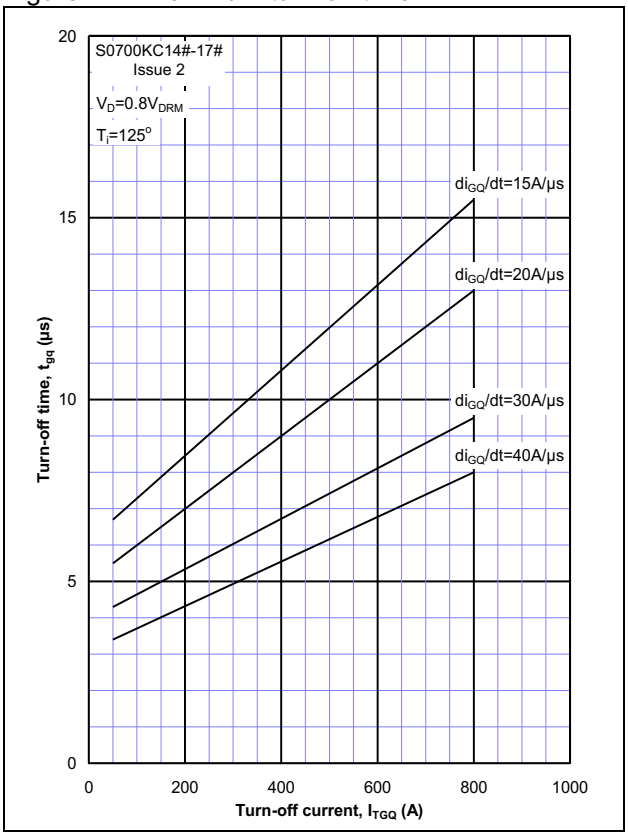


Figure 13 – Turn-off energy per pulse

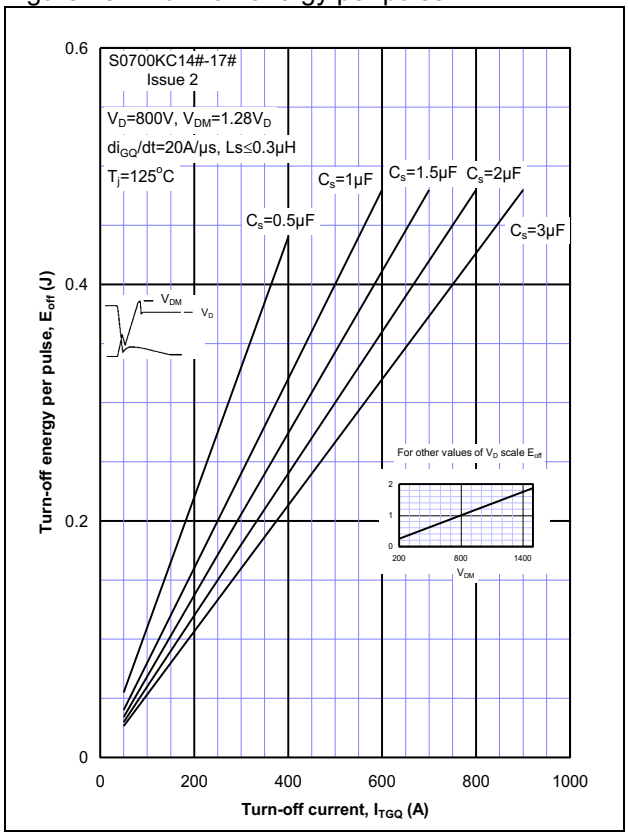


Figure 14 – Typical turn-off energy per pulse

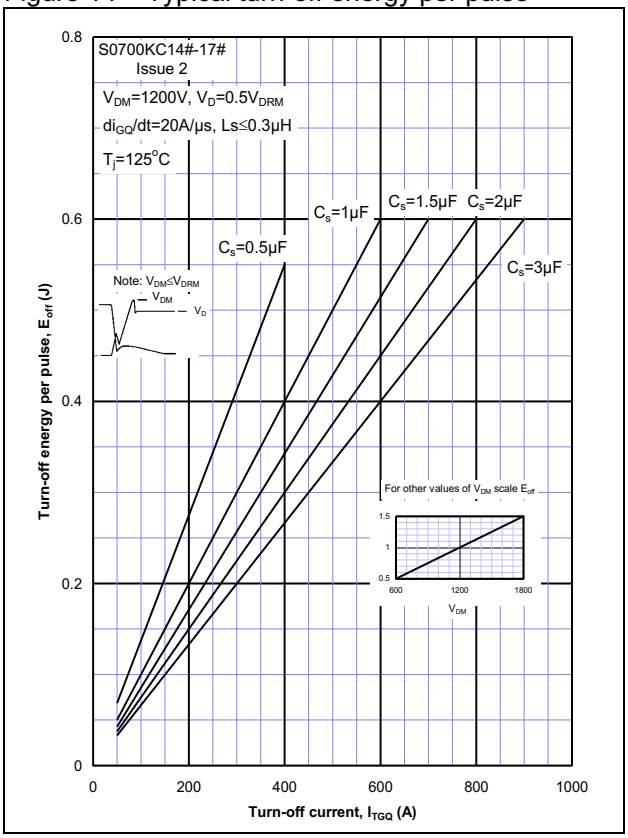


Figure 15 – Maximum permissible turn-off current

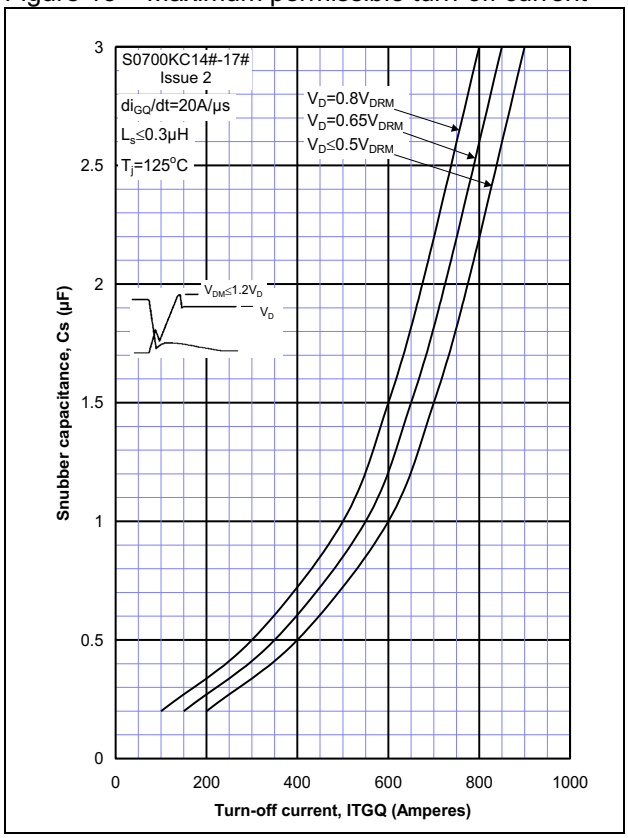


Figure 16 – Maximum turn-off current

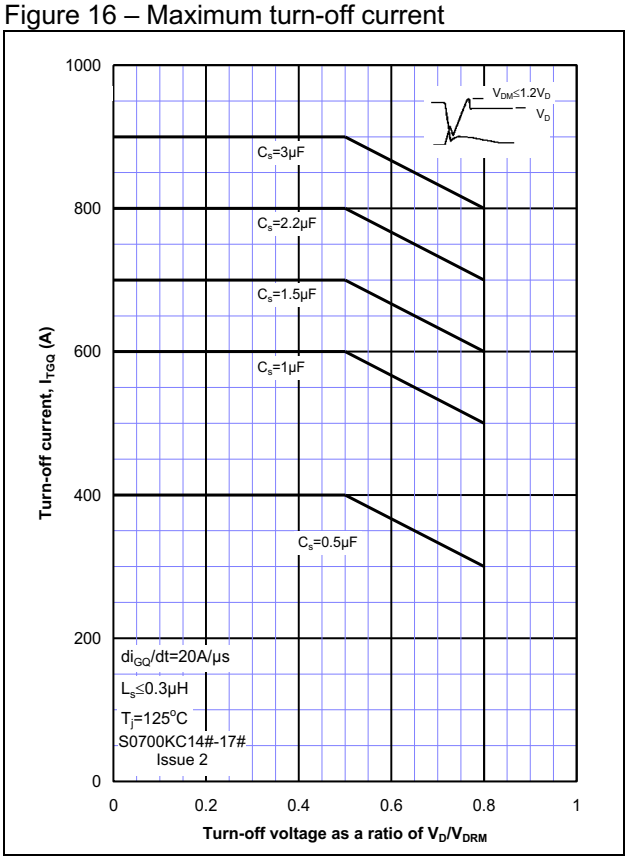


Figure 17 – Maximum tail time

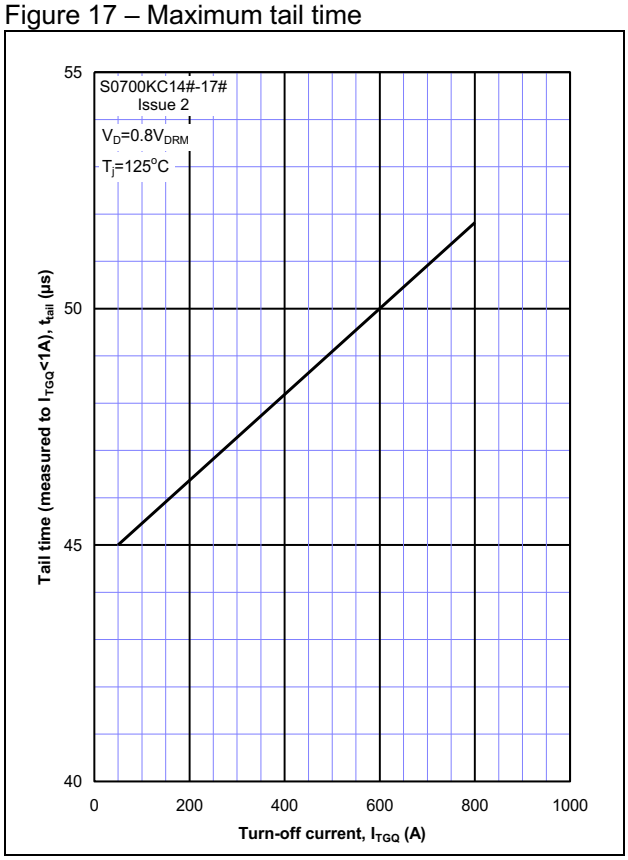
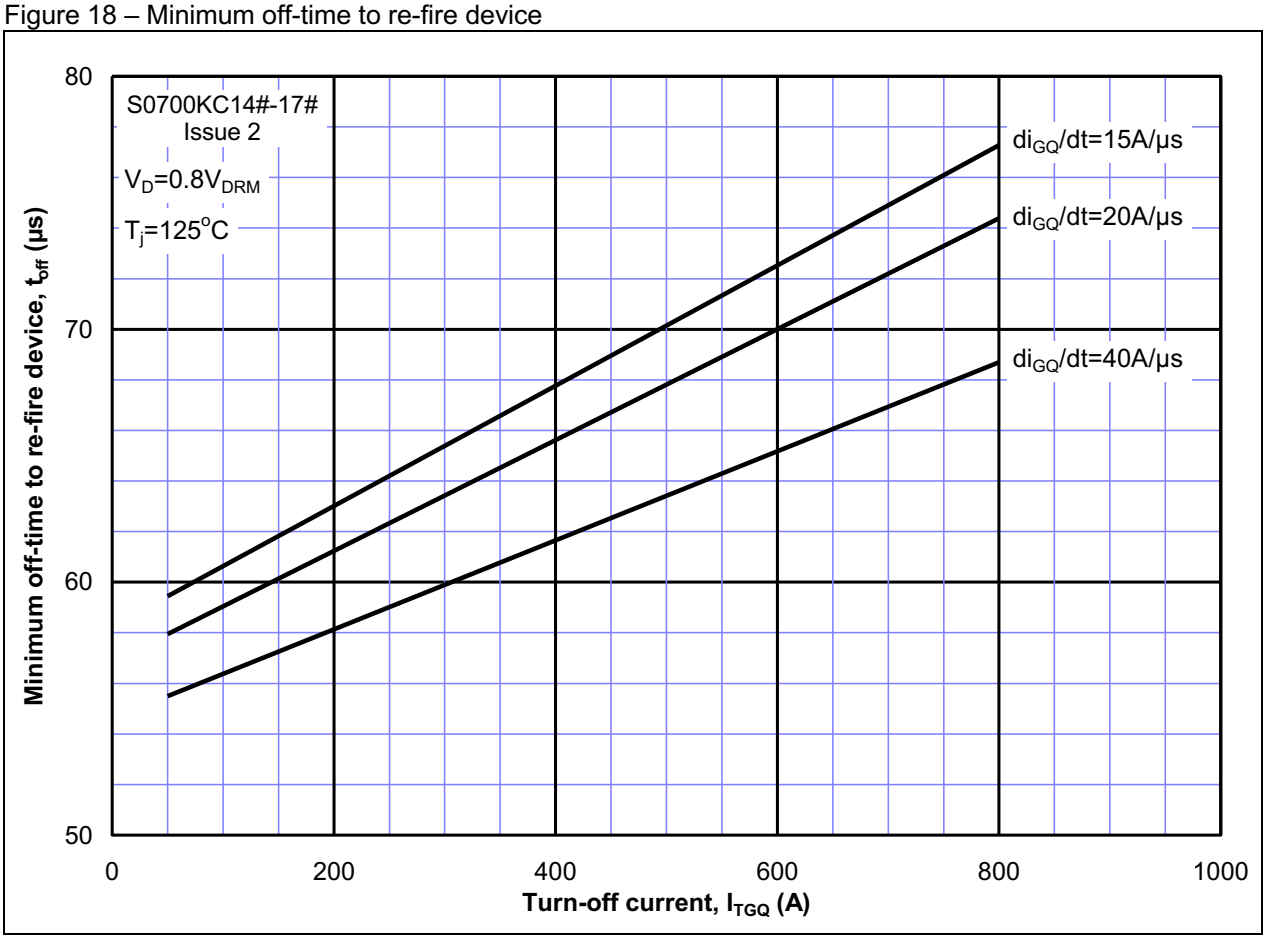
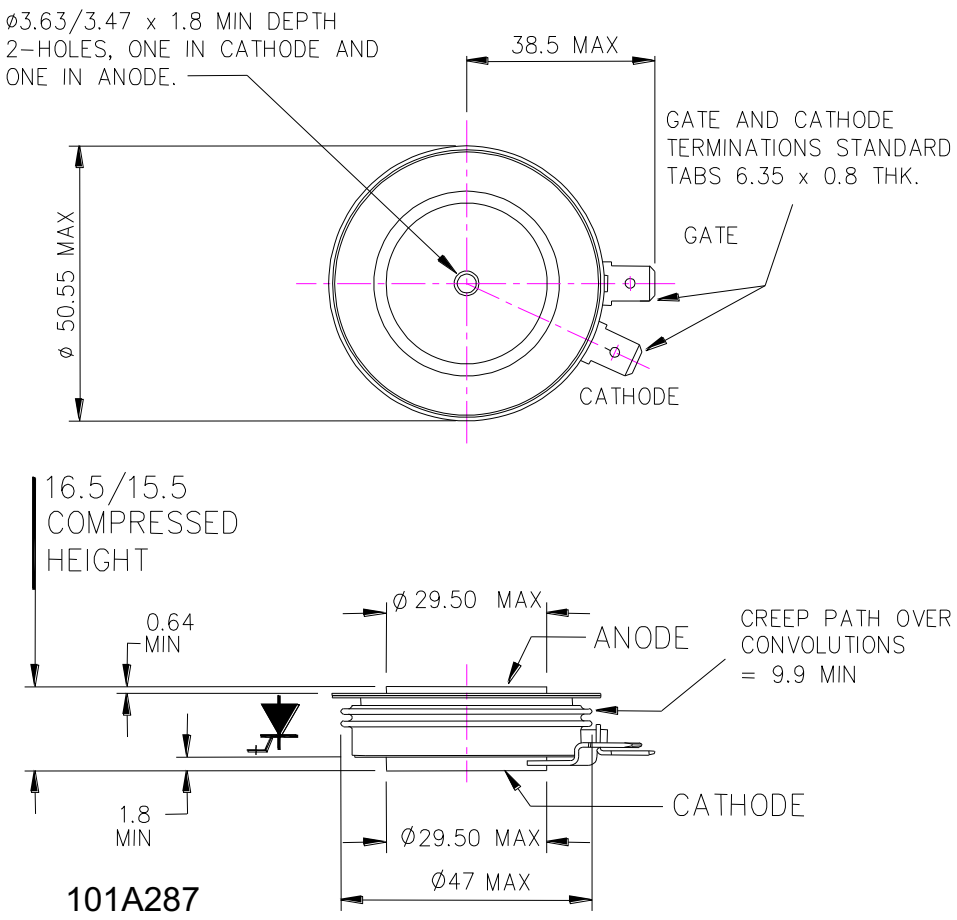


Figure 18 – Minimum off-time to re-fire device



Outline Drawing & Ordering Information



ORDERING INFORMATION (Please quote 10 digit code as below)

S0700	KC	♦♦#
Fixed Type Code	Fixed Outline Code	Voltage Code 140 = 1400V V_{DRM} / V_{RRM} 14Y = 1400V V_{DRM}, 100V V_{RRM} 17D = 1700V V_{DRM}, 1400V V_{RRM} 17Y = 1700V V_{DRM}, 100V V_{RRM}

Typical order code: S0700KC17D – 1700V V_{DRM}, V_{RRM}=80%V_{DRM} (1400V), 16.5mm clamp height capsule.

IXYS Semiconductor GmbH
Edisonstraße 15
D-68623 Lampertheim
Tel: +49 6206 503-0
Fax: +49 6206 503-627
E-mail: marcom@ixys.de

IXYS Corporation
1590 Buckeye Drive
Milpitas CA 95035-7418
Tel: +1 (408) 457 9000
Fax: +1 (408) 496 0670
E-mail: sales@ixys.net

IXYS UK Westcode Ltd
Langley Park Way, Langley Park,
Chippenham, Wiltshire, SN15 1GE.
Tel: +44 (0)1249 444524
Fax: +44 (0)1249 659448
E-mail: sales@ixysuk.com

IXYS Long Beach
IXYS Long Beach, Inc
2500 Mira Mar Ave, Long Beach
CA 90815
Tel: +1 (562) 296 6584
Fax: +1 (562) 296 6585
E-mail: service@ixyslongbeach.com

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