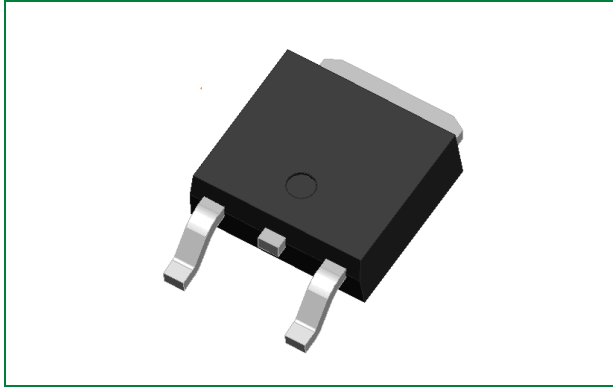


LGD18N40ATH

400 V, 18 A N-Channel Ignition IGBT

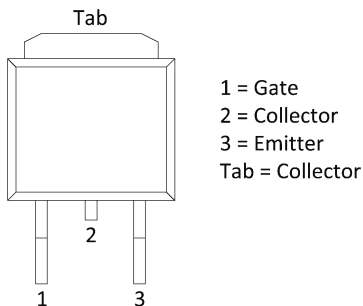


Agency Approvals

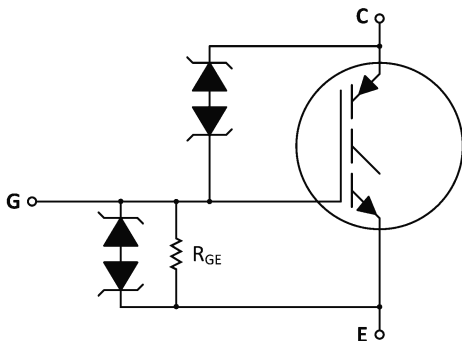
Environmental Approvals



Pinout Diagram



Functional Diagram



Product Summary

Characteristic	Value	Unit
V_{CES}	400	V
I_C	18	A

Description

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil-on-Plug Applications
- DPAK Package Offers Smaller Footprint for Increased Board Space
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage Interfaces Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Optional Gate Resistor (R_G) and Gate-Emitter Resistor (R_{GE})
- AEC-Q101 Qualified
- These are Pb-Free Devices
- Emitter Ballasting for Short-Circuit Capability

1. Maximum Ratings ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)	3
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1. Maximum Ratings ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Conditions	Symbol	Value	Unit
Collector-Emitter Voltage	-	V_{CES}	430	V_{DC}
Collector-Gate Voltage	-	V_{CER}	430	V_{DC}
Gate-Emitter Voltage	-	V_{GE}	18	V_{DC}
Collector Current – Continuous	$T_C = 25^\circ\text{C}$	I_C	15	A_{DC}
Collector Current – Pulsed			50	A_{AC}
ESD – Human Body Model	$R = 1500\ \Omega, C = 100\ \text{pF}$	ESD	8.0	kV
ESD – Machine Model	$R = 0\ \Omega, C = 200\ \text{pF}$		800	V
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	115	W
	Derating for $> 25^\circ\text{C}$		0.77	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	-	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$

2. Unclamped Collector-to-Emitter Avalanche Characteristics

Characteristic	Symbol	Value	Unit
Single Pulse Collector-to-Emitter Avalanche Energy			
$V_{CC} = 50\ \text{V}, V_{GE} = 5.0\ \text{V}, P_{kL} = 21.1\ \text{A}, L = 1.8\ \text{mH}, \text{Starting } T_J = 25^\circ\text{C}$	E_{AS}	400	mJ
$V_{CC} = 50\ \text{V}, V_{GE} = 5.0\ \text{V}, P_{kL} = 16.2\ \text{A}, L = 3.0\ \text{mH}, \text{Starting } T_J = 25^\circ\text{C}$		400	
$V_{CC} = 50\ \text{V}, V_{GE} = 5.0\ \text{V}, P_{kL} = 18.3\ \text{A}, L = 1.8\ \text{mH}, \text{Starting } T_J = 125^\circ\text{C}$		300	
Reverse Avalanche Energy			
$V_{CC} = 100\ \text{V}, V_{GE} = 20\ \text{V}, P_{kL} = 18.3\ \text{A}, L = 6.0\ \text{mH}, \text{Starting } T_J = 150^\circ\text{C}$	$E_{AS(R)}$	2000	mJ

Note: $-55^\circ \leq T_J \leq 150^\circ\text{C}$

3. Maximum Short-Circuit Times

Characteristic	Symbol	Value	Unit
Short Circuit Withstand Time ¹	$t_{sc,1}$	750	μs
Short Circuit Withstand Time ²	$t_{sc,2}$	5.0	ms

Note: $-55^\circ \leq T_J \leq 150^\circ\text{C}$

Footnote 1: See Figure 17, 3 pulses with 10 ms period

Footnote 2: See Figure 18, 3 pulses with 10 ms period

4. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient (DPAK) ³	$R_{\theta JA}$	95	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Footnote 3: When surface mounted to an FR4 board using the minimum recommended pad size

5. Electrical Characteristics – Off

Characteristic	Symbol	Conditions	Temperature	Value			Unit
				Min	Typ	Max	
Collector-Emitter Clamp Voltage	BV _{CES}	I _C = 2.0 mA	T _J = -40 °C to 150 °C	380	395	420	V _{DC}
		I _C = 10 mA		390	405	430	
Zero Gate Voltage Collector Current	I _{CES}	V _{CE} = 15 V, V _{GE} = 0 V	T _J = 25 °C	-	-	2.0	μA _{DC}
			T _J = 150 °C	-	2.0	20	
		V _{CE} = 350 V, V _{GE} = 0 V	T _J = 150 °C	-	10	40 ⁴	
			T _J = -40 °C	-	1.0	10	
Reverse Collector-Emitter Leakage Current	I _{ECS}	V _{CE} = -24 V	T _J = 25 °C	-	0.7	1.0	mA
			T _J = 150 °C	-	12	25 ⁴	
			T _J = -40 °C	-	0.1	1.0	
Reverse Collector-Emitter Clamp Voltage	BV _{CES(R)}	I _C = -75 mA	T _J = 25 °C	27	33	37	V _{DC}
			T _J = 150 °C	30	36	40	
			T _J = -40 °C	25	32	35	
Gate-Emitter Clamp Voltage	BV _{GES}	I _G = 5.0 mA	T _J = -40 °C to 150 °C	11	13	15	V _{DC}
Gate-Emitter Leakage Current	I _{GES}	V _{GE} = 10 V	T _J = -40 °C to 150 °C	384	640	700	μA _{DC}
Gate-Emitter Resistor	R _{GE}	-	T _J = -40 °C to 150 °C	10	16	26	kΩ
Gate Resistor	R _G	-	T _J = -40 °C to 150 °C	-	70	-	Ω

Footnote 4: Maximum Value of Characteristic across Temperature Range

6. Electrical Characteristics – On

Characteristic	Symbol	Conditions	Temperature	Value			Unit
				Min	Typ	Max	
Gate Threshold Voltage	V _{GE(th)}	I _C = 1.0 mA, V _{GE} = V _{CE}	T _J = 25 °C	1.1	1.4	1.9	V _{DC}
			T _J = 150 °C	0.75	1.0	1.4	
			T _J = -40 °C	1.2	1.6	2.1 ⁴	
Threshold Temperature Coefficient (Negative)	-	-	-	-	3.4	-	mV/°C
Collector-Emitter On-Voltage ⁵	V _{CE(on)}	I _C = 6.0 A, V _{GE} = 4.0 V	T _J = 25 °C	1.0	1.4	1.6	V _{DC}
			T _J = 150 °C	0.9	1.3	1.6	
			T _J = -40 °C	1.1	1.45	1.7 ⁴	
		I _C = 8.0 A, V _{GE} = 4.0 V	T _J = 25 °C	1.3	1.6	1.9 ⁴	
			T _J = 150 °C	1.2	1.55	1.8	
			T _J = -40 °C	1.4	1.6	1.9 ⁴	
		I _C = 10.0 A, V _{GE} = 4.0 V	T _J = 25 °C	1.4	1.8	2.05	
			T _J = 150 °C	1.4	1.8	2.0	
			T _J = -40 °C	1.4	1.8	2.1 ⁴	
		I _C = 15 A, V _{GE} = 4.0 V	T _J = 25 °C	1.8	2.2	2.5	
			T _J = 150 °C	2.0	2.4	2.6 ⁴	
			T _J = -40 °C	1.7	2.1	2.5	
		I _C = 10 A, V _{GE} = 4.5 V	T _J = 25 °C	1.3	1.8	2.0 ⁴	
			T _J = 150 °C	1.3	1.75	2.0 ⁴	
			T _J = -40 °C	1.4	1.8	2.0 ⁴	
I _C = 6.5 A, V _{GE} = 3.7 V	T _J = 25 °C	-	-	1.65			
Forward Transconductance ⁵	gfs	V _{CS} = 5.0 V, I _C = 6.0 A	T _J = -40 °C to 150 °C	8.0	14	25	Mhos

Footnote 4: Maximum Value of Characteristic across Temperature Range

Footnote 5: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

7. Dynamic Characteristics

Characteristic	Symbol	Conditions	Temperature	Value			Unit
				Min	Typ	Max	
Input Capacitance	C_{ISS}	$V_{CC} = 25\text{ V}, V_{GE} = 0\text{ V},$ $f = 1.0\text{ MHz}$	$T_J = -40\text{ }^\circ\text{C to } 150\text{ }^\circ\text{C}$	400	800	1000	pF
Output Capacitance	C_{OSS}			50	75	100	
Transfer Capacitance	C_{RSS}			4	7	10	

8. Switching Characteristics

Characteristic	Symbol	Conditions	Temperature	Value			Unit
				Min	Typ	Max	
Turn-off Delay Time (Resistive)	$t_{d(off)}$	$V_{CC} = 300\text{ V}, I_C = 6.5\text{ A},$ $R_G = 1.0\text{ k}\Omega, R_L = 46\text{ }\Omega$	$T_J = 25\text{ }^\circ\text{C}$	-	4.0	10	μs
Fall Time (Resistive)	t_f			-	9.0	15	
Turn-on Delay Time	$t_{d(on)}$	$V_{CC} = 10\text{ V}, I_C = 6.5\text{ A},$ $R_G = 1.0\text{ k}\Omega, R_L = 1.5\text{ }\Omega$	$T_J = 25\text{ }^\circ\text{C}$	-	0.7	4.0	μs
Rise Time	t_r			-	4.5	7.0	

9. Figure Data

Figure 1. Output Characteristics ($T_J = 25\text{ }^\circ\text{C}$)

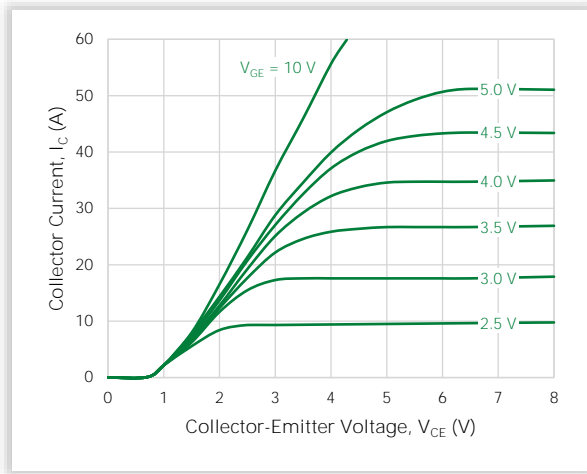


Figure 2. Output Characteristics ($T_J = -40\text{ }^\circ\text{C}$)

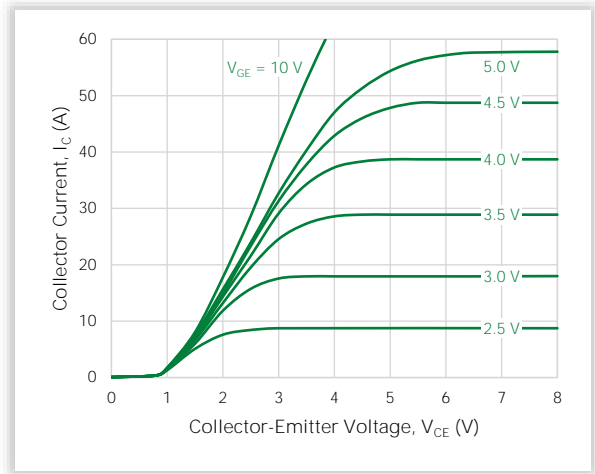


Figure 3. Output Characteristics ($T_J = 150\text{ }^\circ\text{C}$)

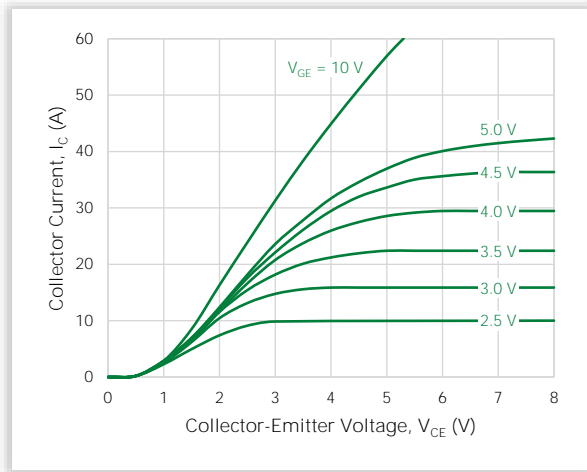


Figure 4. Transfer Characteristics

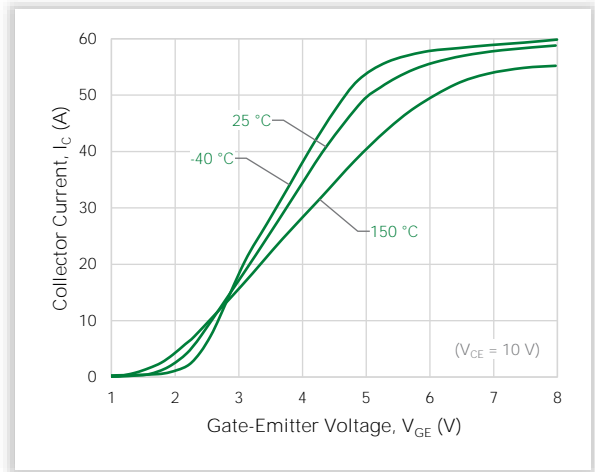


Figure 5. Collector-Emitter Saturation Voltage vs. Junction Temperature

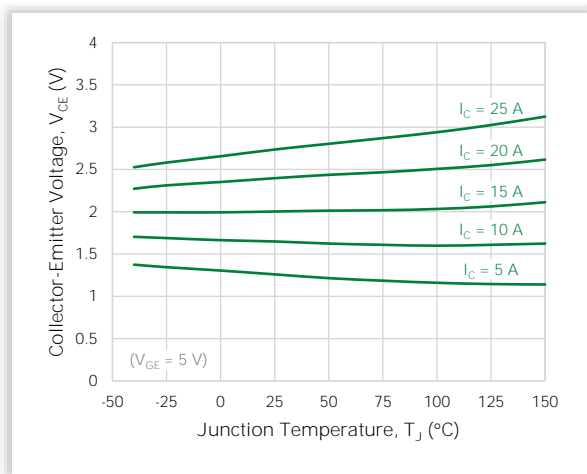


Figure 6. Collector-Emitter Voltage vs. Gate-Emitter Voltage ($T_J = 25\text{ }^\circ\text{C}$)

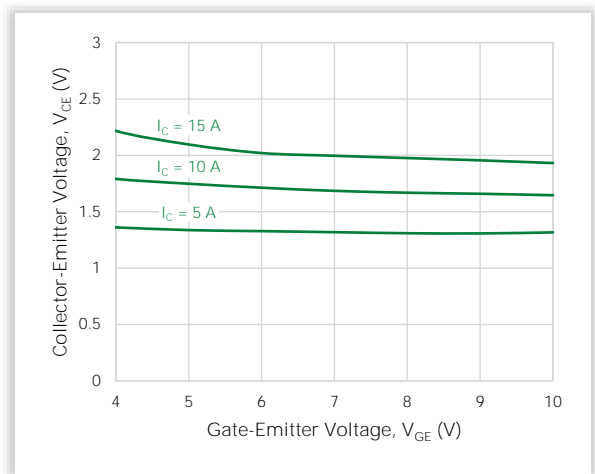


Figure 7. Collector-Emitter Voltage vs. Gate-Emmitter Voltage ($T_J = 150\text{ }^\circ\text{C}$)

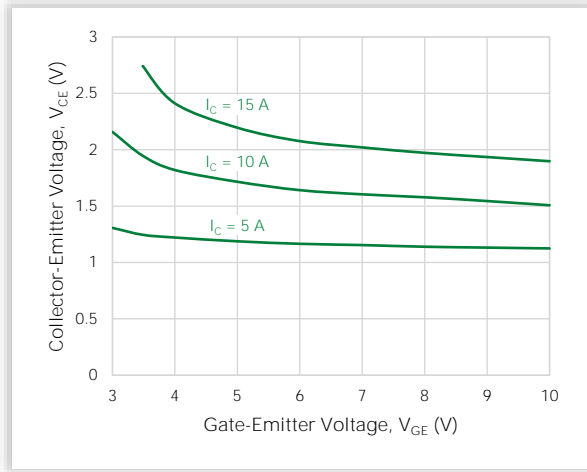


Figure 8. Capacitance Variation

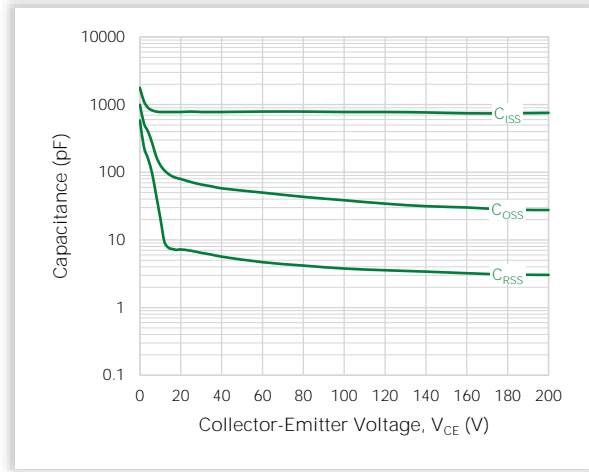


Figure 9. Gate Threshold Voltage vs. Temperature

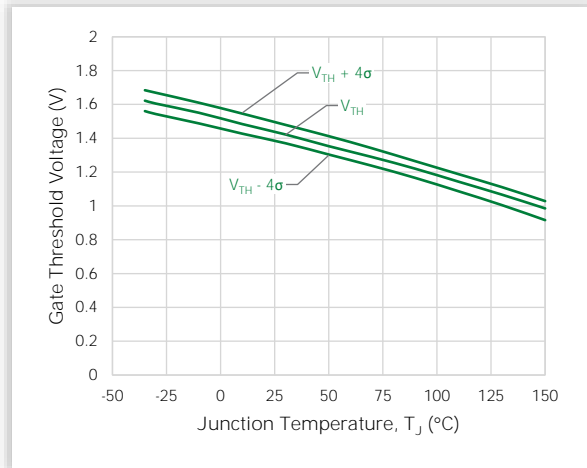


Figure 10. Minimum Open Secondary Latch Current vs. Temperature

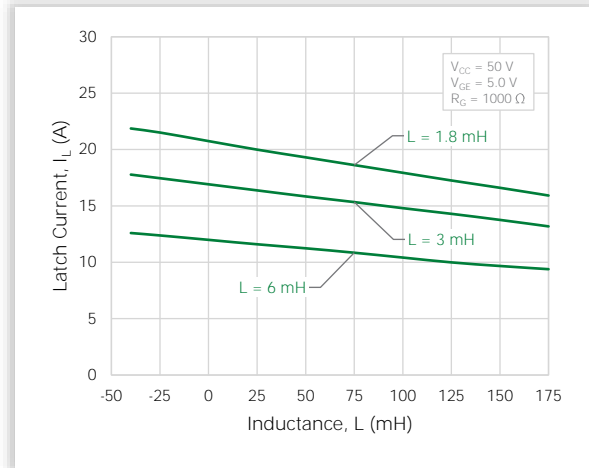


Figure 11. Typical Open Secondary Latch Current vs. Temperature

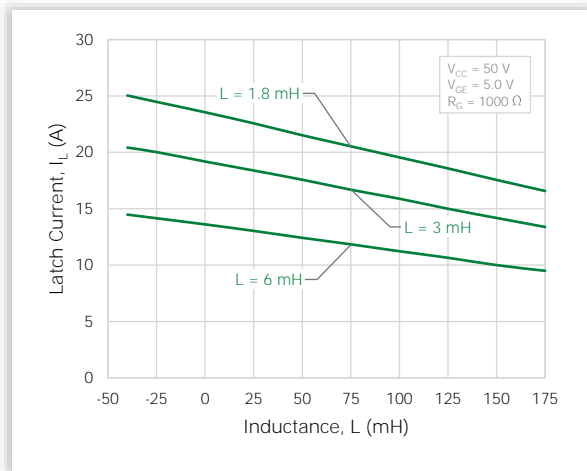


Figure 12. Inductive Switching Fall Time vs. Temperature

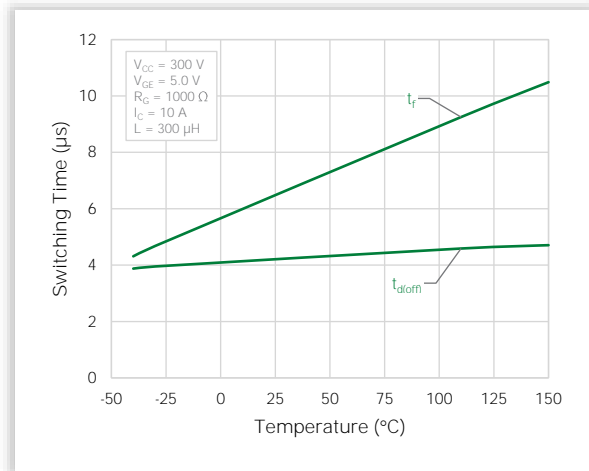


Figure 13. Single Pulse Safe Operating Area
(Mounted on an Infinite Heatsink at $T_A = 25^\circ\text{C}$)

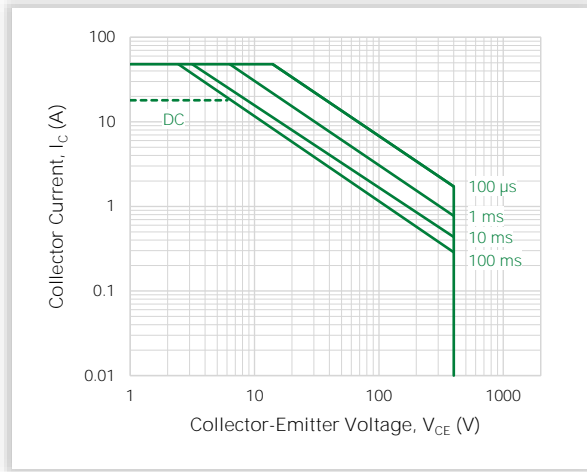


Figure 14. Single Pulse Safe Operating Area
(Mounted on an Infinite Heatsink at $T_A = 125^\circ\text{C}$)

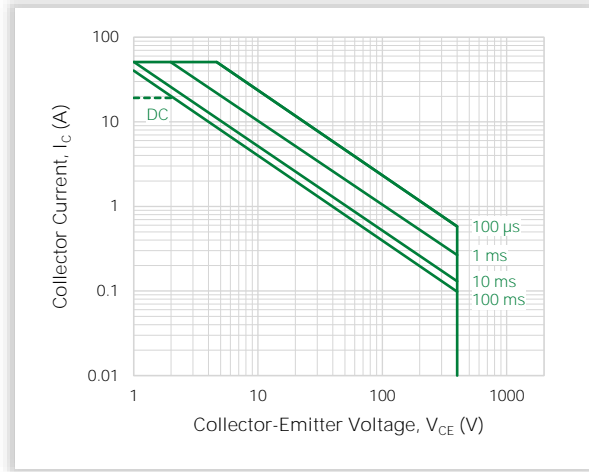


Figure 15. Pulse Train Safe Operating Area
(Mounted on an Infinite Heatsink at $T_A = 25^\circ\text{C}$)

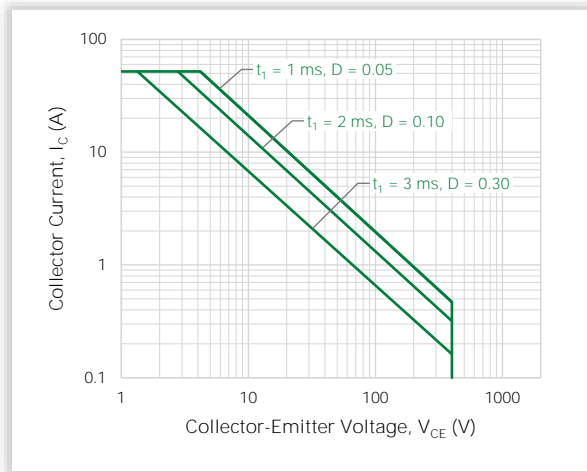


Figure 16. Pulse Train Safe Operating Area
(Mounted on an Infinite Heatsink at $T_A = 125^\circ\text{C}$)

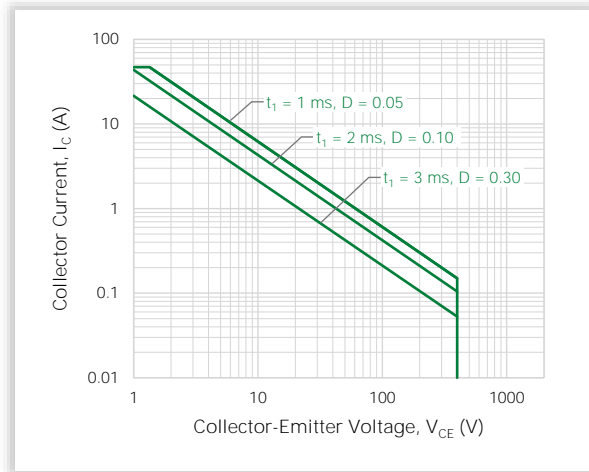


Figure 17. Circuit Configuration for Short Circuit Test 1

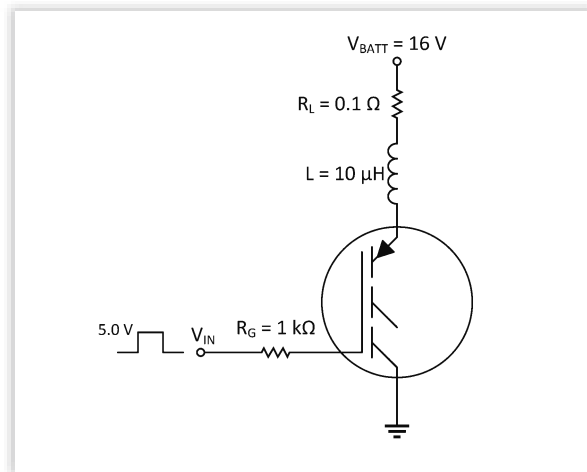


Figure 18. Circuit Configuration for Short Circuit Test 2

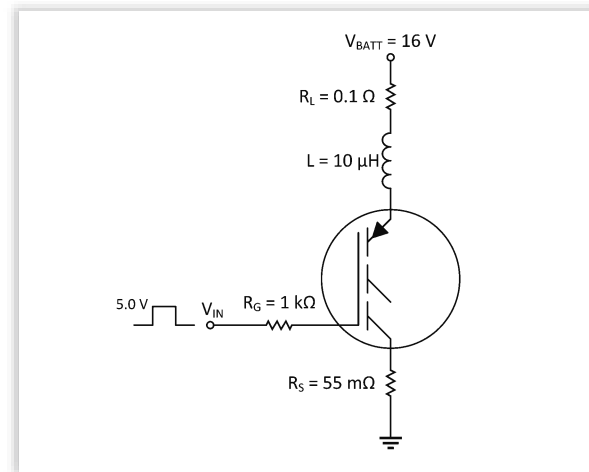
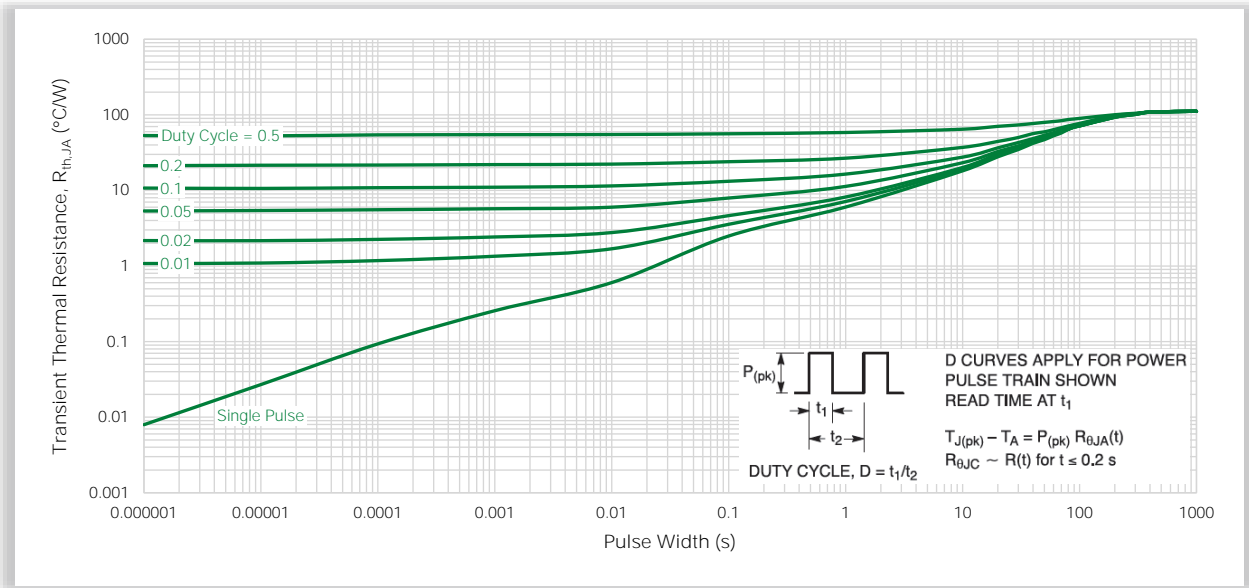
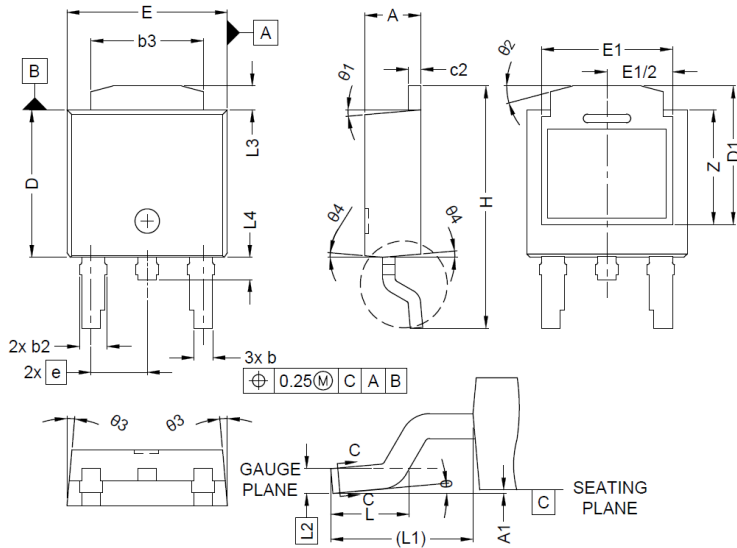


Figure 19. Transient Thermal Resistance

(Non-normalized Junction-Ambient mounted on minimum pad area)

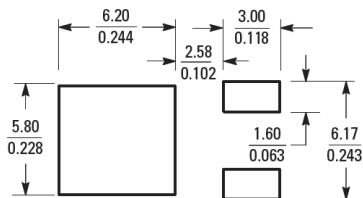


10. Package Dimensions



Symbol	Millimeters		
	Min	Nom	Max
A	2.18	-	2.38
A1	0.00	-	0.13
b	0.63	-	0.89
b2	0.72	-	1.14
b3	4.57	-	5.46
c	0.46	-	0.61
c2	0.46	-	0.61
D	5.97	-	6.22
D1	5.45	-	5.85
E	6.35	-	6.73
E1	5.14	-	5.54
e	2.29 BSC		
H	9.40	-	10.41
L	1.40	-	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	-	1.27
L4	-	-	1.01
Z	3.93	-	-
theta	0°	-	10°
theta1	0°	-	10°
theta2	10°	-	20°
theta3	0°	-	10°
theta4	0°	-	10°

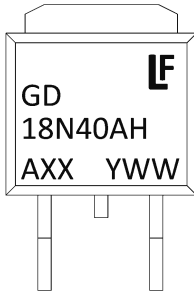
Recommended Solder Pad Layout:



Notes:

1. DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. HEAT SINK SIDE FLASH IS MAX. 0.8mm .
4. RADIUS ON TERMINAL IS OPTIONAL.

11. Part Numbering and Marking



GD18N40AH = Device Code
 A = Assembly Location
 XX = Lot Number
 Y = Year
 WW = Work Week
 H = Ballast Structure Design

12. Packing Options

Part Number	Package	Packing Mode	M.O.Q.
LGD18N40ATH	DPAK (Pb-Free)	Tape & Reel	2500

For additional information please visit www.Littelfuse.com/powersemi

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